

## Model Name: GA-H61M-D2P-B3

Revision 1.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*4 SLOT
16	ASM1085/1083
17	PCI SLOT1&2
18	ITE 8728 LPC IO
19	COM,KB_USB,USB_ESATA,-PROCHOT
20	HWM,FAN CTRL,OV,
21	DUAL BIOS
22	FP,FUSB,SPK,SATALED
23	CODEC ALC889
24	REAR AUDIO JACK
25	REALTEK RTL8111E(VL)
26	DVI
27	DISCRETE POWER

SHEET

TITLE

28	ATX,-S_WARN,-S_ACK,5VDUAL1
29	ISL95870_CPU_VTT
30	VCORE ISL6364_1
31	VCORE ISL6364_2
32	VCORE ISL6364_3
33	TPM,COMB,LPT

**Gigabyte Technology**

Cover Sheet

Size Custom	Document Number <b>GA-H61M-D2P-B3</b>	Rev <b>1.0</b>
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Revision 1.0

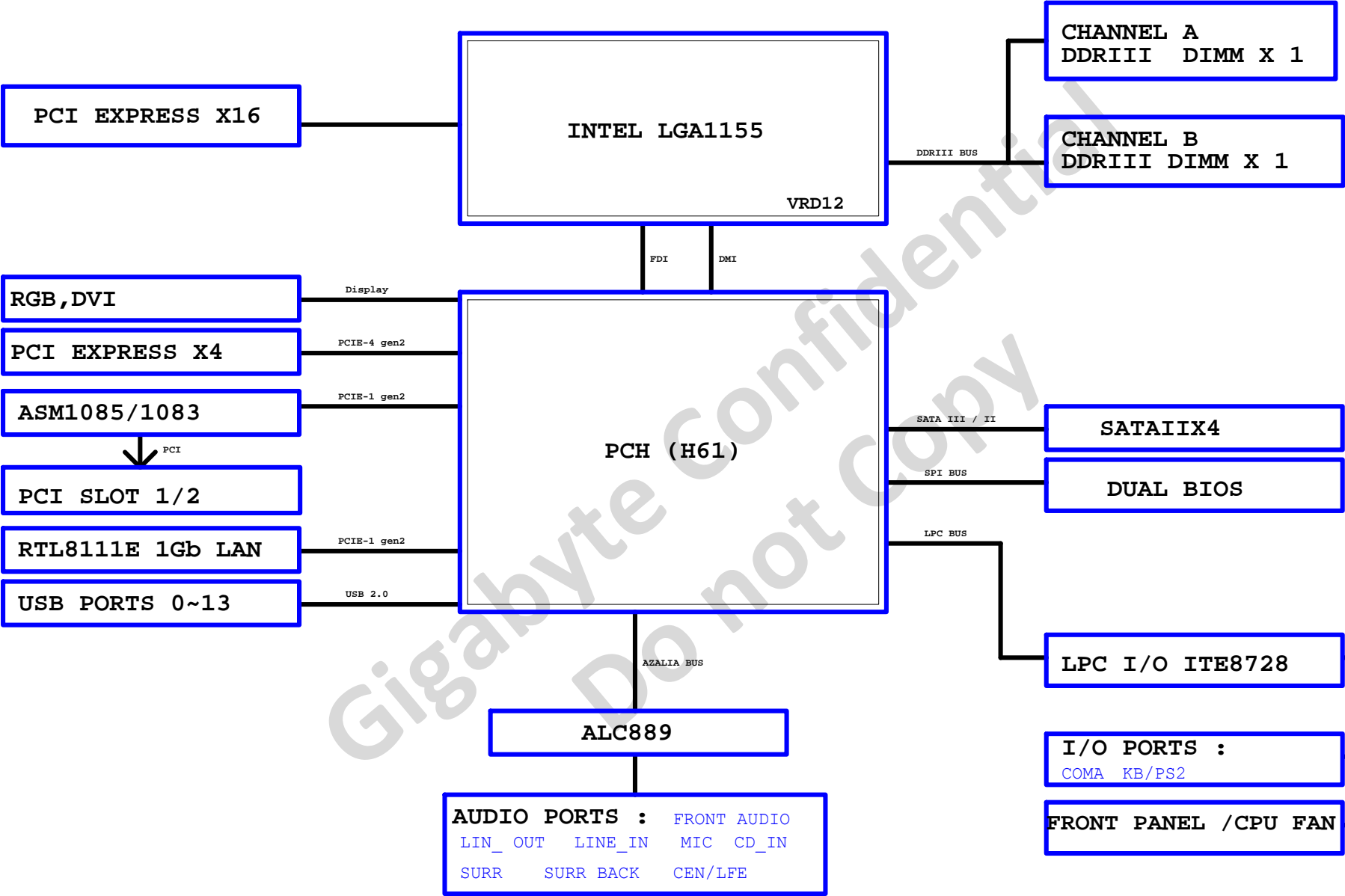
## Circuit or PCB layout change

## Component value change history

2011/02/16

[illegible][illegible]

BLOCK DIAGRAM





## CPUA

MAAA0	AV27	SA_MA[0]	SA_DQS[0]	AK3	DQSA0
MAAA1	AY24	SA_MA[1]	SA_DQS[0]	AK2	-DQSA0
MAAA2	AW24	SA_MA[2]			
MAAA3	AV23	SA_MA[3]			
MAAA4	AV23	SA_MA[3]	SA_DQ[0]	AJ3	MDA0
MAAA5	AT24	SA_MA[4]	SA_DQ[1]	AJ4	MDA1
MAAA6	AT23	SA_MA[5]	SA_DQ[2]	AL3	MDA2
MAAA7	AV22	SA_MA[6]	SA_DQ[3]	AL4	MDA3
MAAA8	AU22	SA_MA[7]	SA_DQ[4]	AJ2	MDA4
MAAA9	AT22	SA_MA[8]	SA_DQ[5]	AJ1	MDA5
MAAA10	AV28	SA_MA[9]	SA_DQ[6]	AL2	MDA6
MAAA11	AU21	SA_MA[10]	SA_DQ[7]	AL1	MDA7
MAAA12	AT21	SA_MA[11]			
MAAA13	AW32	SA_MA[12]	SA_DQS[1]	AP3	DQSA1
MAAA14	AU20	SA_MA[13]	SA_DQS[1]	AP2	-DQSA1
MAAA15	AT20	SA_MA[14]			

[7]	-SWEA	AW29	SA_WE#	SA_DQ[8]	AN1	MDA8
[7]	-SCASA	AV30	SA_CAS#	SA_DQ[9]	AN4	MDA9
[7]	-SRASA	AU28	SA_RAS#	SA_DQ[10]	AR3	MDA10

[7]	SBA00	AY29	SA_BS[0]	SA_DQ[11]	AR4	MDA12
[7]	SBA01	AW28	SA_BS[1]	AN2	MDA11	
[7]	SBA02	AV20	SA_BS[2]	AN3	MDA13	
				AR2	MDA14	
				AR1	MDA15	

[7]	-CSA0	AY29	SA_CS#0	SA_DQS[2]	AW4	DQSA2
[7]	-CSA1	AV32	SA_CS#1	SA_DQS[2]	AV4	-DQSA2
		AX30	SA_CS#2			
		AX33	SA_CS#3			

[7]	CKEA0	AV19	SA_CKE[0]	SA_DQ[16]	AV2	MDA16
[7]	CKEA1	AT19	SA_CKE[1]	SA_DQ[17]	AW3	MDA17
		AU18	SA_CKE[2]	SA_DQ[18]	AV5	MDA18
		AV18	SA_CKE[3]	SA_DQ[19]	AV5	MDA19

	MODT_A0	AV31	SA_ODT[0]	SA_DQ[20]	AU2	MDA20
	MODT_A1	AU32	SA_ODT[1]	SA_DQ[21]	AU3	MDA21
		AX30	SA_ODT[2]	SA_DQ[22]	AY5	MDA22
		AX33	SA_ODT[3]	SA_DQ[23]	AY5	MDA23

[7]	DCLKA0	AY25	SA_CLK[0]	SA_DQS[3]	AV8	DQSA3
[7]	-DCLKA0	AW25	SA_CLK[0]	SA_DQS[3]	AW8	-DQSA3
[7]	DCLKA1	AU24	SA_CLK[1]			
[7]	-DCLKA1	AU25	SA_CLK[1]			

	AY27	SA_CLK[2]	SA_DQ[24]	AJ7	MDA24	
	AY27	SA_CLK[2]	SA_DQ[25]	AJ7	MDA25	
	AY26	SA_CLK[3]	SA_DQ[26]	AV9	MDA26	
	AY26	SA_CLK[3]	SA_DQ[27]	AU9	MDA27	
	AY26	SA_CLK[3]	SA_DQ[28]	AV7	MDA28	
	AY26	SA_CLK[3]	SA_DQ[29]	AV7	MDA29	
	AY26	SA_CLK[3]	SA_DQ[30]	AV9	MDA30	
	AY26	SA_CLK[3]	SA_DQ[31]	AY9	MDA31	

[7,8]	-DDR3_RST	AW18	SM_DRAMRST#			
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C89  
0.1u/4X7R/16V/K/X

	AV13	SA_DQS[8]				
	AV12	SA_DQS[8]				
	AU12	SA_ECC_CB[0]				
	AU14	SA_ECC_CB[1]				
	AU13	SA_ECC_CB[2]				
	AY13	SA_ECC_CB[3]				
	AU13	SA_ECC_CB[4]				
	AU11	SA_ECC_CB[5]				
	AY12	SA_ECC_CB[6]				
	AW12	SA_ECC_CB[7]				

	AR40	MDA40				
	AR37	MDA41				
	SA_DQ[41]	AN38	MDA42			
	SA_DQ[42]	AN37	MDA43			
	SA_DQ[43]	AR39	MDA44			
	SA_DQ[44]	AR38	MDA45			
	SA_DQ[45]	AN38	MDA46			
	SA_DQ[46]	AN40	MDA47			
	SA_DQ[47]					

	AK38	DQSA6				
	AK39	-DQSA6				

	SA_DQ[48]	AL40	MDA48			
	SA_DQ[49]	AL37	MDA49			
	SA_DQ[50]	AJ38	MDA50			
	SA_DQ[51]	AJ37	MDA51			
	SA_DQ[52]	AL39	MDA52			
	SA_DQ[53]	AL38	MDA53			
	SA_DQ[54]	AJ39	MDA54			
	SA_DQ[55]	AJ40	MDA55			

	SA_DQS[7]	AF38	DQSA7			
	SA_DQS[7]	AF39	-DQSA7			

	SA_DQ[56]	AG40	MDA56			
	SA_DQ[57]	AG37	MDA57			
	SA_DQ[58]	AE38	MDA58			
	SA_DQ[59]	AE37	MDA59			
	SA_DQ[60]	AG39	MDA60			
	SA_DQ[61]	AG38	MDA61			
	SA_DQ[62]	AE39	MDA62			
	SA_DQ[63]	AE40	MDA63			

DDR\_0

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LGA1155[10SC1-F01155-01R\_10SC1-F01155-02R]

## CPUB

MAAB0	AK24	SB_MA[0]	SB_DQS[0]	AH7	DQSB0
MAAB1	AM20	SB_MA[1]	SB_DQS[0]	AH6	-DQSB0
MAAB2	AM19	SB_MA[2]			
MAAB3	AK18	SB_MA[3]			
MAAB4	AP19	SB_MA[4]	SB_DQ[0]	AG7	MDB0
MAAB5	AP18	SB_MA[5]	SB_DQ[1]	AG8	MDB1
MAAB6	AM18	SB_MA[6]	SB_DQ[2]	AJ9	MDB2
MAAB7	AL18	SB_MA[7]	SB_DQ[3]	AJ8	MDB3
MAAB8	AN18	SB_MA[8]	SB_DQ[4]	AG5	MDB4
MAAB9	AY17	SB_MA[9]	SB_DQ[5]	AG6	MDB5
MAAB10	AN23	SB_MA[10]	SB_DQ[6]	AJ6	MDB6
MAAB11	AU17	SB_MA[11]	SB_DQ[7]	AJ7	MDB7
MAAB12	AT18	SB_MA[12]			
MAAB13	AR26	SB_MA[13]	SB_DQS[1]	AM8	DQSB1
MAAB14	AY16	SB_MA[14]	SB_DQS[1]	AL8	-DQSB1
MAAB15	AV16	SB_MA[15]			

[8]	-SWEB	AR25	SB_WE#	SB_DQ[8]	AL7	MDB8
[8]	-SCASB	AK25	SB_CAS#	SB_DQ[9]	AM7	MDB9
[8]	-SRASB	AP24	SB_RAS#	SB_DQ[10]	AM10	MDB10

[8]	SBAB0	AP23	SB_BS[0]	SB_DQ[11]	AL6	MDB11
[8]	SBAB1	AW17	SB_BS[1]	SB_DQ[12]	AM6	MDB12
[8]	SBAB2	AW17	SB_BS[2]	SB_DQ[13]	AL9	MDB13

[8]	-CSB0	AN25	SB_CS#0	SB_DQ[14]	AM9	MDB15
[8]	-CSB1	AN25	SB_CS#1	SB_DQ[15]		
		AN26	SB_CS#2			
		AX26	SB_CS#2			
		AX26	SB_CS#3			

[8]	CKEB0	AU18	SB_CKE[0]	SB_DQ[16]	AP7	MDB16
[8]	CKEB1	AY16	SB_CKE[1]	SB_DQ[17]	AR7	MDB17
		AW15	SB_CKE[2]	SB_DQ[18]	AP10	MDB18
		AV15	SB_CKE[3]	SB_DQ[19]	AR10	MDB19

	MODT_B0	AL26	SB_ODT[0]	SB_DQ[20]	AP6	MDB20
	MODT_B1	AP26	SB_ODT[1]	SB_DQ[21]	AP9	MDB21
		AM26	SB_ODT[2]	SB_DQ[22]	AR6	MDB22
		AK26	SB_ODT[3]	SB_DQ[23]	AR9	MDB23

		AV8	SB_DQS[3]	AN13	DQSB3	
		AW8	SB_DQS[3]	AN12	-DQSB3	

[8]	DCLKB0	AL21	SB_CLK[0]	SB_DQ[24]	AM12	MDB24
[8]	-DCLKB0	AL22	SB_CLK[0]	SB_DQ[25]	AM13	MDB25
[8]	DCLKB1	AL20	SB_CLK[1]	SB_DQ[26]	AR13	MDB26
[8]	-DCLKB1	AK20	SB_CLK[1]	SB_DQ[27]	AP13	MDB27

		AM22	SB_CLK[2]	SB_DQ[28]	AL12	MDB28
		AP21	SB_CLK[2]	SB_DQ[29]	AL13	MDB29
		AN21	SB_CLK[3]	SB_DQ[30]	AR12	MDB30
			SB_CLK[3]	SB_DQ[31]	AP12	MDB31

		AN29	SB_DQS[4]	AN29	DQSB4	
		AN28	SB_DQS[4]	AN28	-DQSB4	

[8]	VREF_D0B	AH1	FC_AH1			
[7]	VREF_D0A	AH4	FC_AH4			

		SA_DQ[32]	AR28	MDB32		
		SA_DQ[33]	AR23	MDB33		
		SA_DQ[34]	AL28	MDB34		
		SA_DQ[35]	AL29	MDB35		
		SA_DQ[36]	AP28	MDB36		
		SA_DQ[37]	AP29	MDB37		
		SA_DQ[38]	AM28	MDB38		
		SA_DQ[39]	AM29	MDB39		

		SA_DQS[5]	AP33	DQSB5		
		SA_DQS[5]	AP33	-DQSB5		

		SA_ECC_CB[0]				
		SA_ECC_CB[1]				
		SA_ECC_CB[2]				
		SA_ECC_CB[3]				
		SA_ECC_CB[4]				
		SA_ECC_CB[5]				
		SA_ECC_CB[6]				
		SA_ECC_CB[7]				

		SA_DQ[40]	AP32	MDB40		
		SA_DQ[41]	AP21	MDB41		
		SA_DQ[42]	AP35	MDB42		
		SA_DQ[43]	AP34	MDB43		
		SA_DQ[44]	AR32	MDB44		
		SA_DQ[45]	AR31	MDB45		
		SA_DQ[46]	AR35	MDB46		
		SA_DQ[47]	AR34	MDB47		

		SA_DQS[6]	AL33	DQSB6		
		SA_DQS[6]	AM33	-DQSB6		

		SA_DQ[48]	AM32	MDB48		
		SA_DQ[49]	AM31	MDB49		
		SA_DQ[50]	AL35	MDB50		
		SA_DQ[51]	AL32	MDB51		
		SA_DQ[52]	AM34	MDB52		
		SA_DQ[53]	AL31	MDB53		
		SA_DQ[54]	AM35	MDB54		
		SA_DQ[55]	AL34	MDB55		

		SA_DQS[7]	AG35	DQSB7		
		SA_DQS[7]	AG34	-DQSB7		

		SA_DQ[56]	AH35	MDB56		
		SA_DQ[57]	AH34	MDB57		
		SA_DQ[58]	AE34	MDB58		
		SA_DQ[59]	AE35	MDB59		
		SA_DQ[60]	AJ35	MDB60		
		SA_DQ[61]	AJ34	MDB61		
		SA_DQ[62]	AE33	MDB62		
		SA_DQ[63]	AE33	MDB63		

		SA_DQ[48]	AM32	MDB48		
		SA_DQ[49]	AM31	MDB49		
		SA_DQ[50]	AL35	MDB50		
		SA_DQ[51]	AL32	MDB51		
		SA_DQ[52]	AM34	MDB52		
		SA_DQ[53]	AL31	MDB53		
		SA_DQ[54]	AM35	MDB54		
		SA_DQ[55]	AL34	MDB55		

		SA_DQS[7]	AG35	DQSB7		
		SA_DQS[7]	AG34	-DQSB7		

		SA_DQ[56]	AH35	MDB56		
		SA_DQ[57]	AH34	MDB57		
		SA_DQ[58]	AE34	MDB58		
		SA_DQ[59]	AE35	MDB59		
		SA_DQ[60]	AJ35	MDB60		
		SA_DQ[61]	AJ34	MDB61		
		SA_DQ[62]	AE33	MDB62		
		SA_DQ[63]	AE33	MDB63		

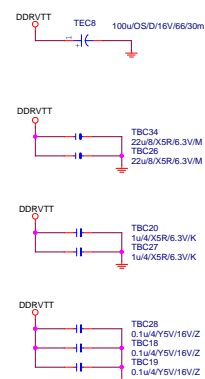
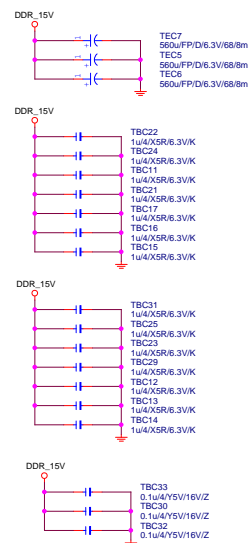
		SA_DQ[48]	AM32	MDB48		
		SA_DQ[49]	AM31	MDB49		
		SA_DQ[50]	AL35	MDB50		
		SA_DQ[51]	AL32	MDB51		
		SA_DQ[52]	AM34	MDB52		
		SA_DQ[53]	AL31	MDB53		
		SA_DQ[54]	AM35	MDB54		
		SA_DQ[55]	AL34	MDB55		

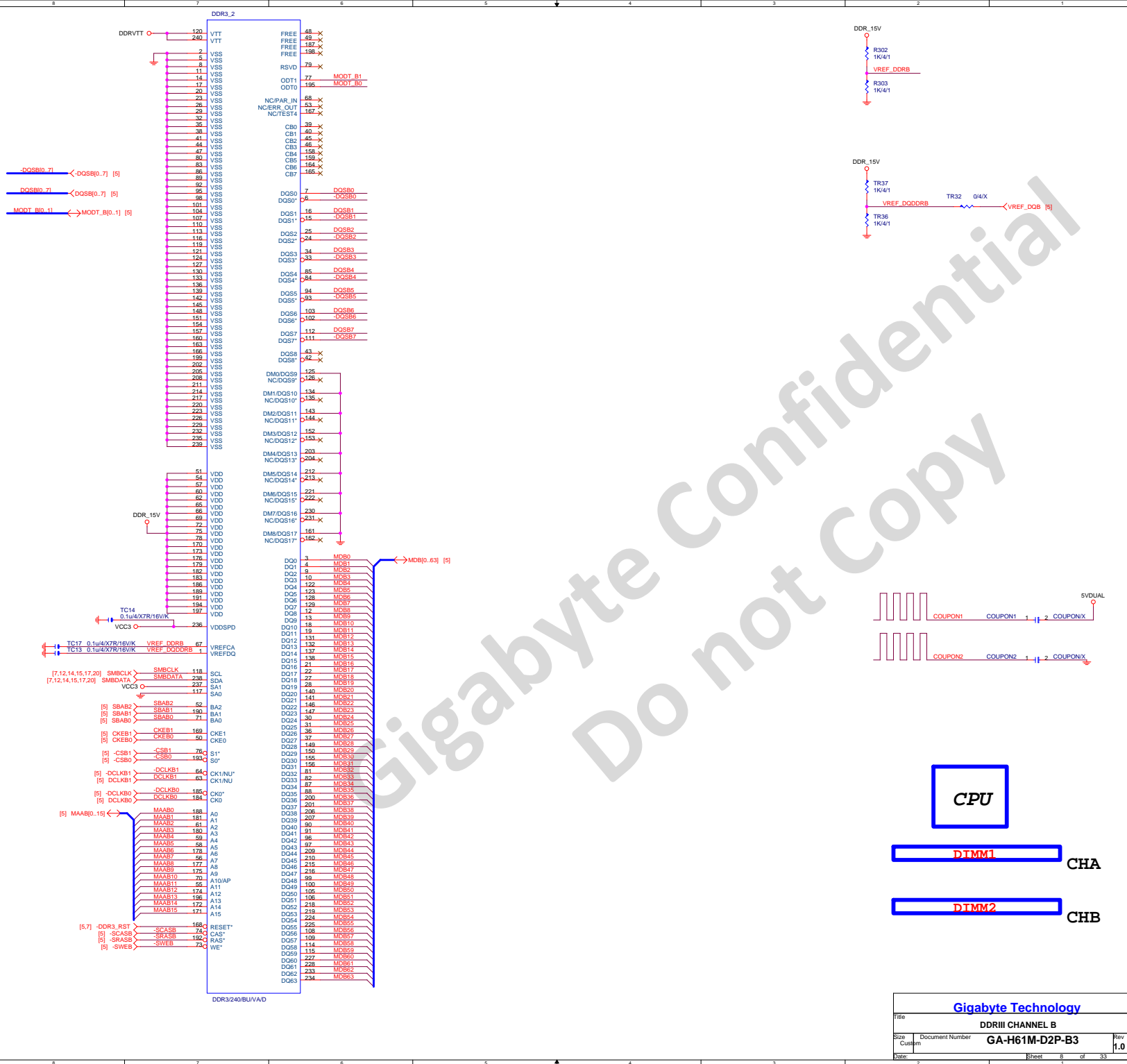
		SA_DQS[7]	AG35	DQSB7		
		SA_DQS[7]	AG34	-DQSB7		

		SA_DQ[56]	AH35	MDB56		
		SA_DQ[57]	AH34	MDB57		
		SA_DQ[58]	AE34	MDB58		
		SA_DQ[59]	AE35	MDB59		
		SA_DQ[60]	AJ35	MDB60		
		SA_DQ[61]	AJ34	MDB61		
		SA_DQ[62]	AF35	MDB62		
		SA_DQ[63]	AF34	MDB63		
		SA_DQ[64]	AF35	MDB64		
		SA_DQ[65]	AF34	MDB65		
		SA_DQ[66]	AF35	MDB66		
		SA_DQ[67]	AF34	MDB67		
		SA_DQ[68]	AF35	MDB68		
		SA_DQ[69]	AF34	MDB69		
		SA_DQ[70]	AF35	MDB70		
		SA_DQ[71]	AF34	MDB71		
		SA_DQ[72]	AF35	MDB72		
		SA_DQ[73]	AF34	MDB73		
		SA_DQ[74]	AF35	MDB74		
		SA_DQ[75]	AF34	MDB75		
		SA_DQ[76]	AF35	MDB76		
		SA_DQ[77]	AF34	MDB77		
		SA_DQ[78]	AF35	MDB78		
		SA_DQ[79]	AF34	MDB79		
		SA_DQ[80]	AF35	MDB80		
		SA_DQ[81]	AF34	MDB81		
		SA_DQ[82]	AF35	MDB82		
		SA_DQ[83]	AF34	MDB83		
		SA_DQ[84]	AF35	MDB84		
		SA_DQ[85]	AF34	MDB85		
		SA_DQ[86]	AF35	MDB86		
		SA_DQ[87]	AF34	MDB87		
		SA_DQ[88]	AF35	MDB88		
		SA_DQ[89]	AF34	MDB89		
		SA_DQ[90]	AF35	MDB90		
		SA_DQ[91]	AF34	MDB91		
		SA_DQ[92]	AF35	MDB92		
		SA_DQ[93]	AF34	MDB93		
		SA_DQ[94]	AF35	MDB94		
		SA_DQ[95]	AF34	MDB95		
		SA_DQ[96]	AF35	MDB96		
		SA_DQ[97]	AF34	MDB97		
		SA_DQ[98]	AF35	MDB98		
		SA_DQ[99]	AF34	MDB99		



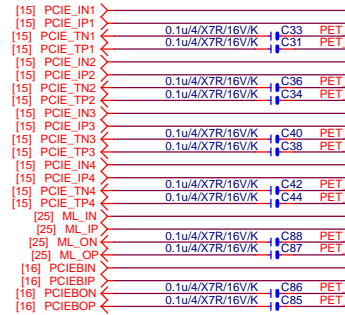






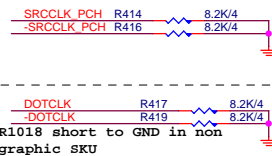


PCHG		FDILINK			
		FDI_RXN0	C42	FDI_TXN0	
TP21		FDI_RXP0	B43	FDI_TXP0	
TP22		FDI_RXN1	F45	FDI_TXN1	
TP29		FDI_RXP1	F43	FDI_TXP1	
TP33		FDI_RXN2	H41	FDI_TXN2	
		FDI_RXP2	J41	FDI_TXP2	
TP22		FDI_RXN3	C46	FDI_TXN3	
TP26		FDI_RXP3	D47	FDI_TXP3	
TP30		FDI_RXN4	B45	FDI_TXN4	
TP34		FDI_RXP4	A46	FDI_TXP4	
		FDI_RXN5	C47	FDI_TXN5	
TP23		FDI_RXP5	C49	FDI_TXP5	
TP27		FDI_RXN6	J43	FDI_TXN6	
TP31		FDI_RXP6	H43	FDI_TXP6	
TP35		FDI_RXN7	M43	FDI_TXN7	
		FDI_RXP7	P43	FDI_TXP7	
TP24					
TP28		FDI_FSYNCO	B51	FDI_FSYNCO	→ FDI_LSYNCO [4]
TP32		FDI_LSYNCO	E49	FDI_LSYNCO	→ FDI_LSYNCO [4]
TP36		FDI_FSYNC1	C52	FDI_FSYNC1	→ FDI_FSYNC1 [4]
		FDI_LSYNC1	D51	FDI_LSYNC1	→ FDI_LSYNC1 [4]
		FDI_INT	H46	FDI_INT	→ FDI_INT [4]



FOR FUSE SHORT GPIO

FDI\_TXP[0..7]      >>> FDI\_TXP[0..7] [4]  
FDI\_TXN[0..7]      >>> FDI\_TXN[0..7] [4]



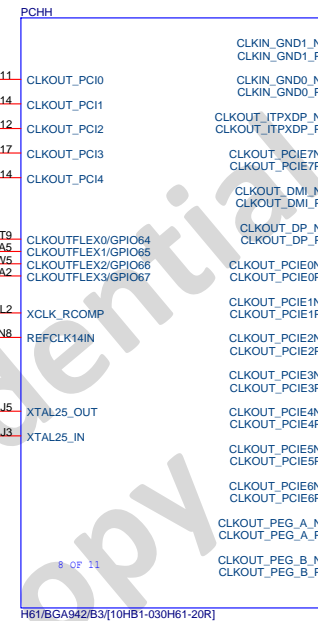
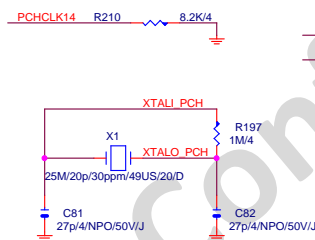
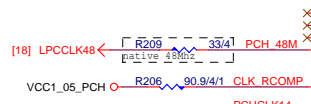
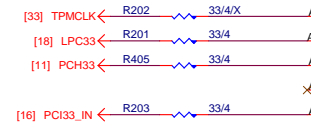
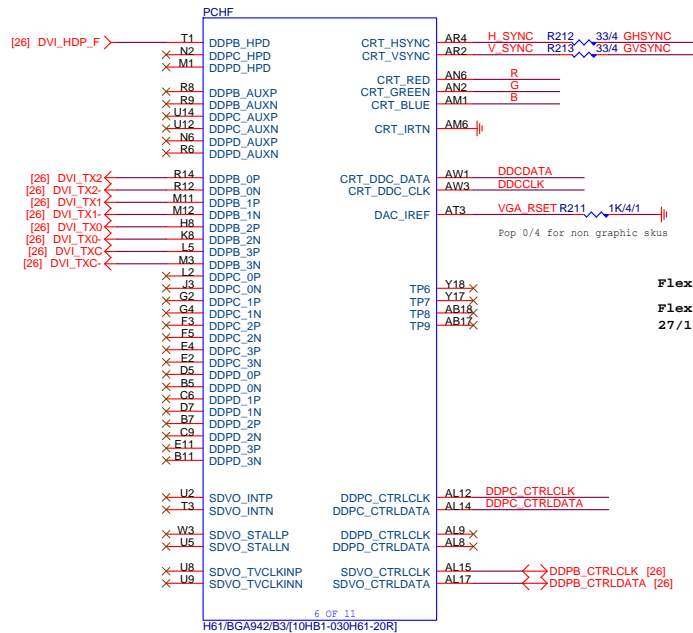
PCHE	
148	RESERVED_29
147	DF_TVS
141	RESERVED_6
150	RESERVED_4
149	RESERVED_3
143	RESERVED_2
157	RESERVED_1
	RESERVED_22
	RESERVED_21
	RESERVED_14
	RESERVED_13
	RESERVED_12
	RESERVED_11
	RESERVED_10
	RESERVED_9
	RESERVED_8
	RESERVED_7
	RESERVED_20
	RESERVED_19
	RESERVED_18
	RESERVED_17
	RESERVED_16
	RESERVED_15
	RESERVED_28
	RESERVED_27
	RESERVED_26
	RESERVED_25
	RESERVED_24
	RESERVED_23
	RESERVED_5

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H61/BGA942/B3/(10HB1-030/H61-20R)

32.4/4/1 for ONFI enable

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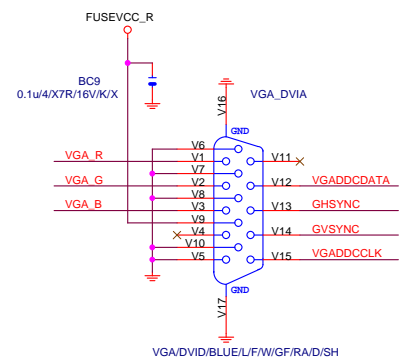
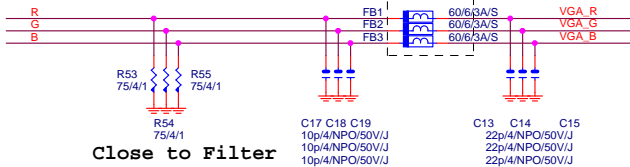
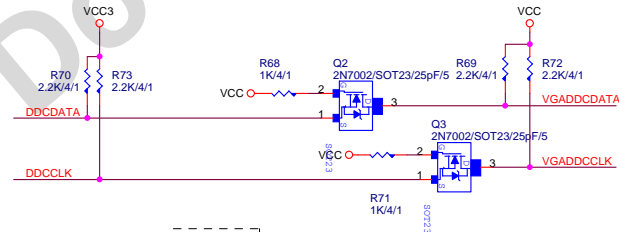
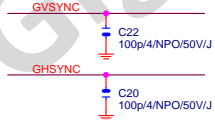
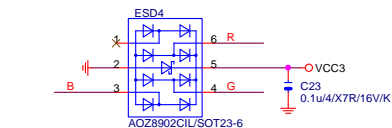
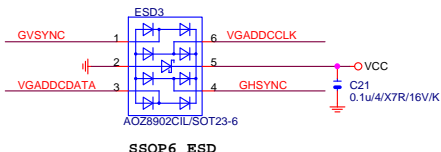
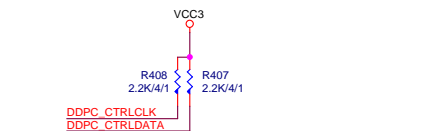


PCIEX4

LAN

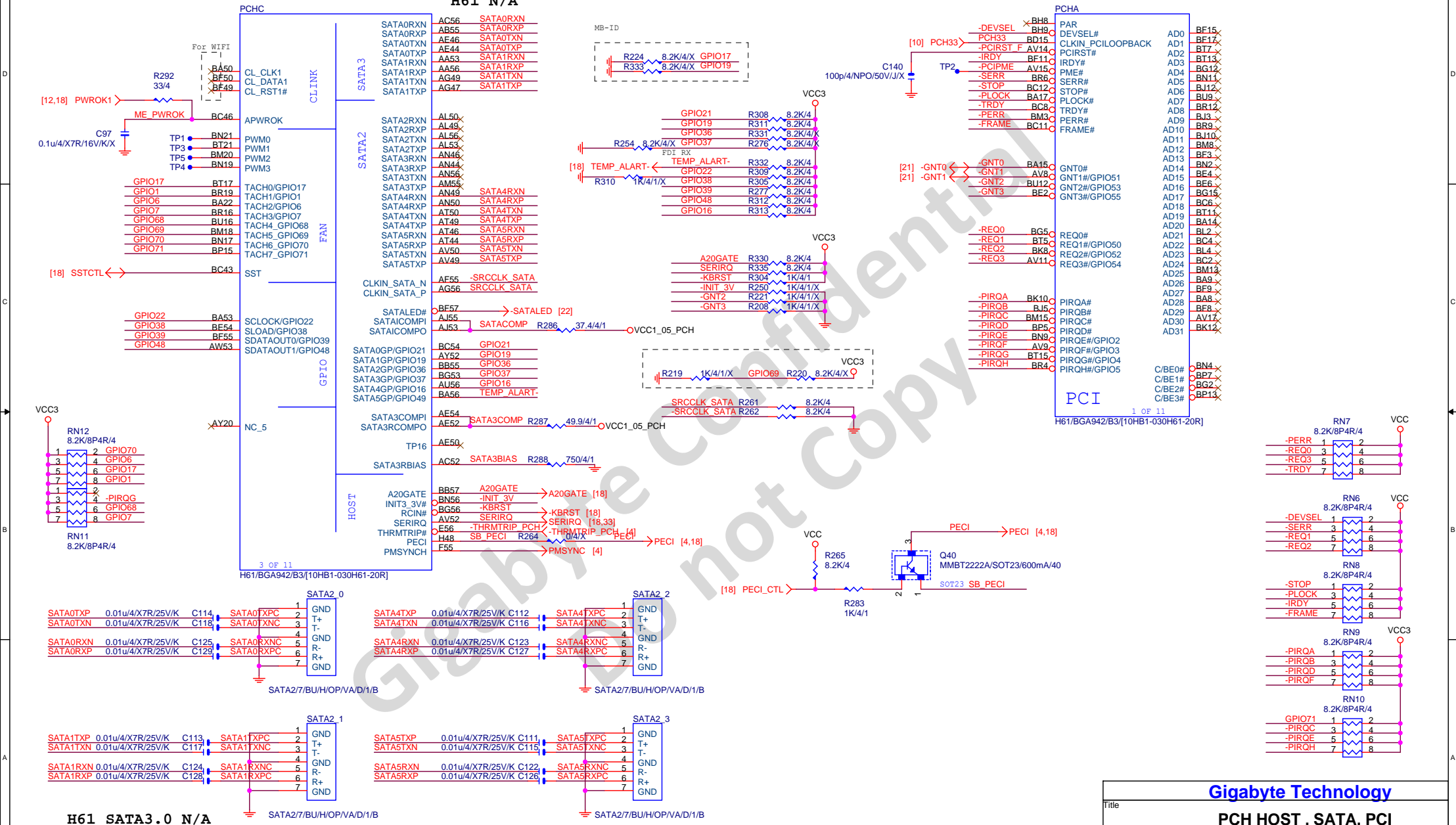
BRIDGE

PCIEX16



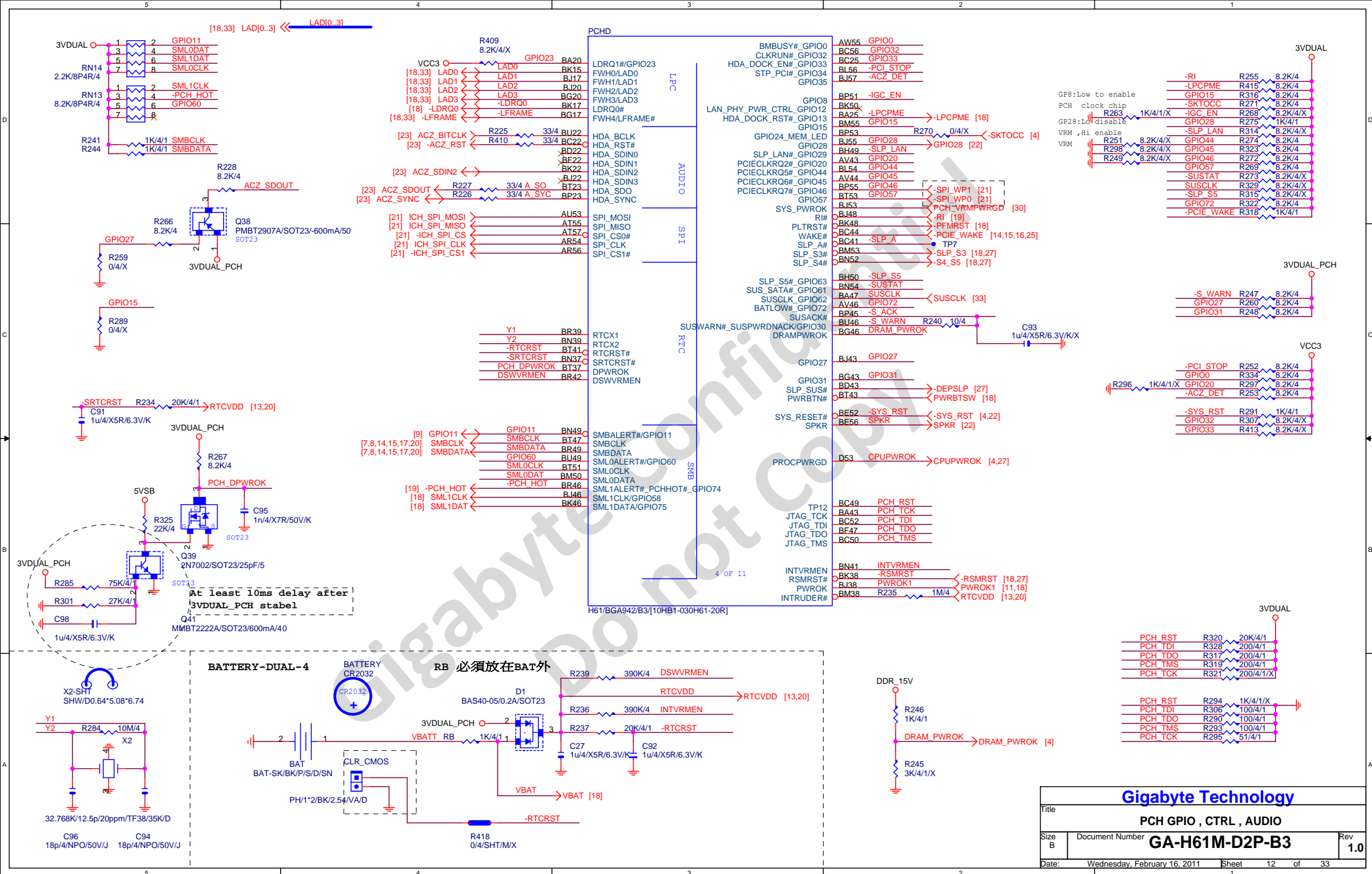
Gigabyte Technology			
PCH DISPLAY, CLK BUFFER			
GA-H61M-D2P-B3			
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Date	Wednesday, February 16, 2011	Sheet	10 of 33

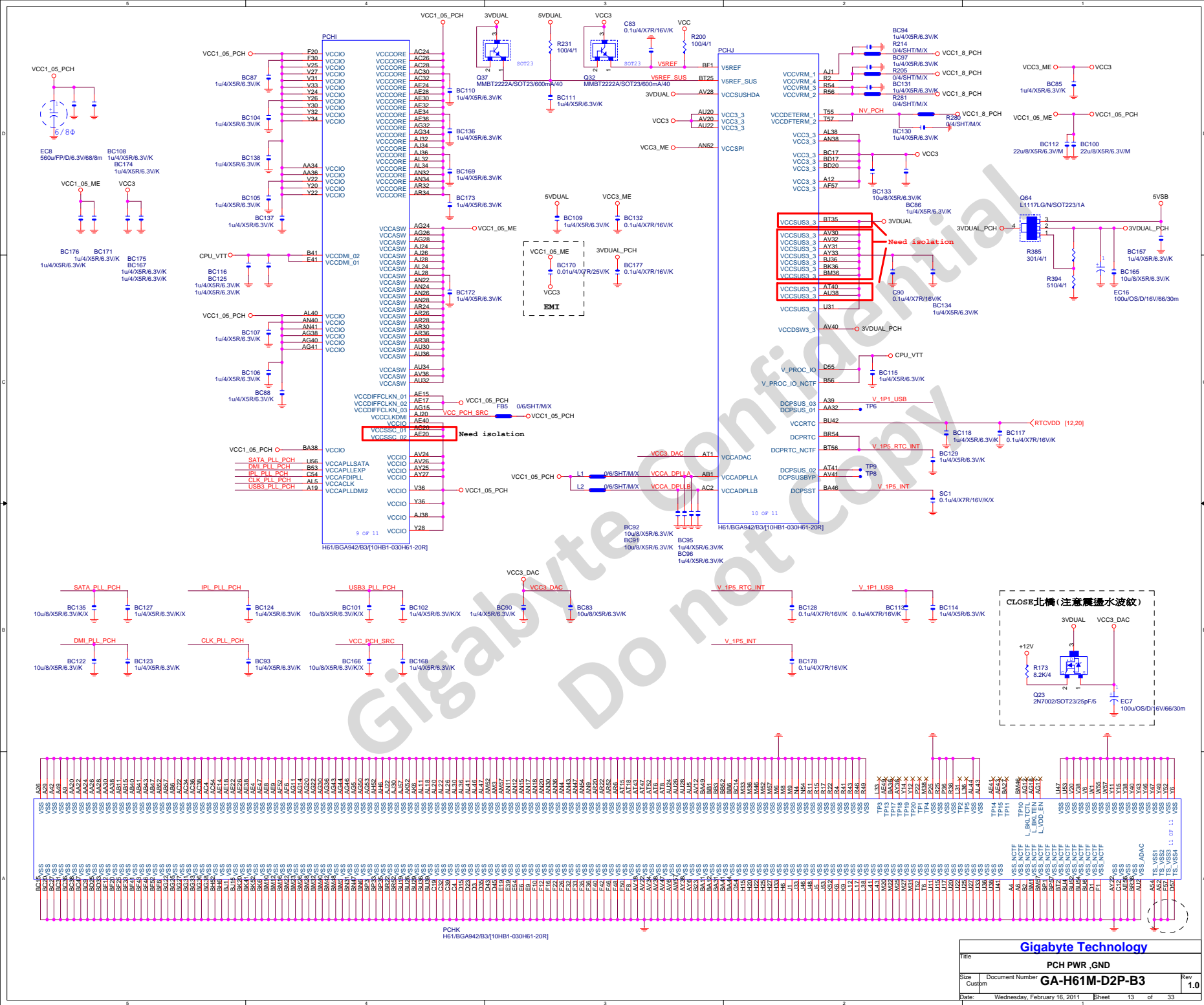
```
B65 SATA3.0 ONLY PORT0
H61 N/A
```



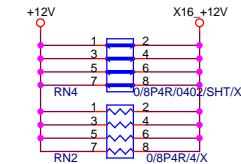
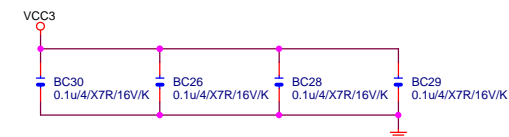
H61 SATA3.0 N/A

H1X7-SATA2-HS-MASK



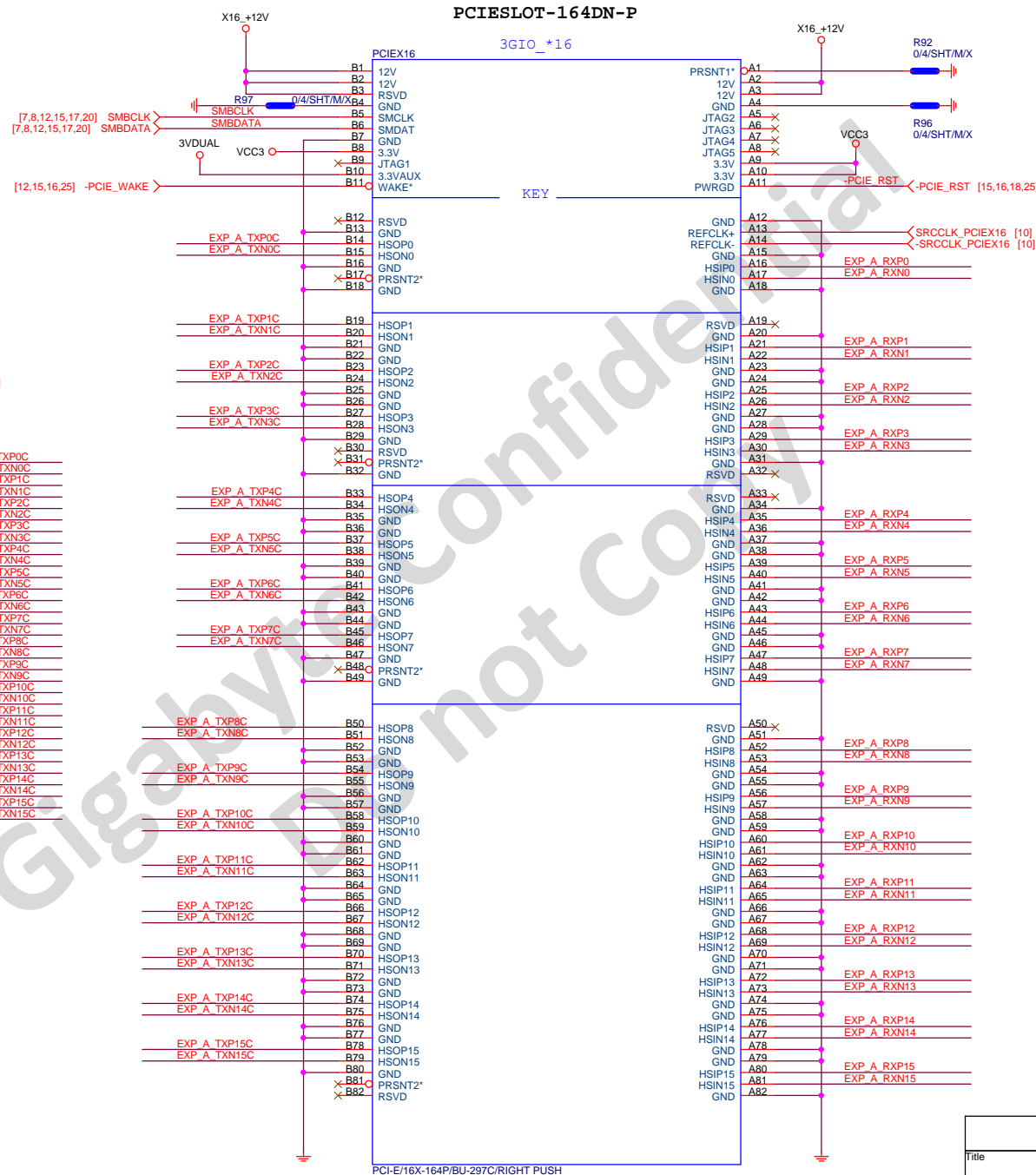




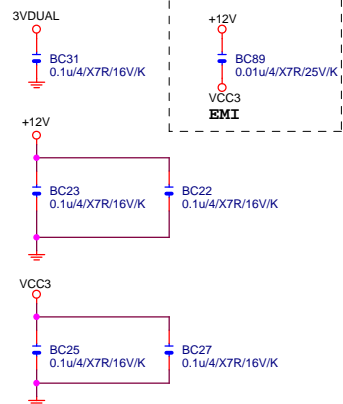
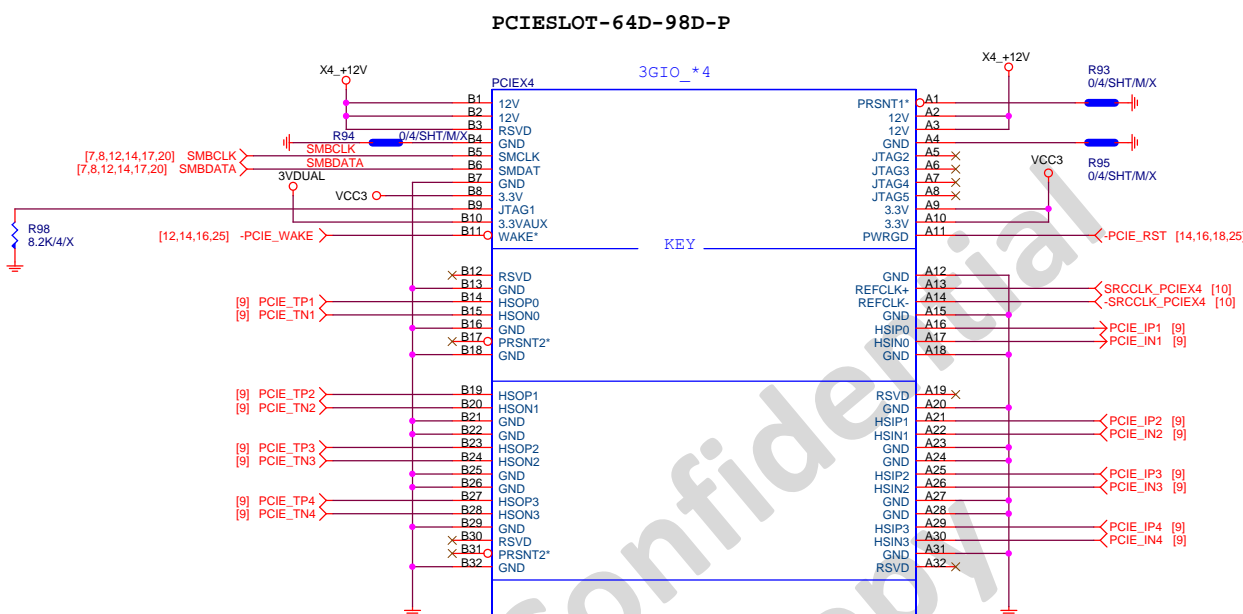
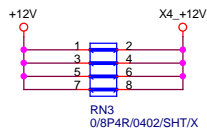


```
EXP A RXP[0..15]    >>EXP_A_RXP[0..15] [4]
EXP A RXN[0..15]    >>EXP_A_RXN[0..15] [4]
EXP A TXP[0..15]    >>EXP_A_TXP[0..15] [4]
EXP A TXN[0..15]    >>EXP_A_TXN[0..15] [4]
```

EXP A TXP0	C32	0.22u4/X5R5/6.3V/K	EXP A TXP0C
EXP A TXN0	C30	0.22u4/X5R5/6.3V/K	EXP A TXN0C
EXP A TXP1	C35	0.22u4/X5R5/6.3V/K	EXP A TXP1C
EXP A TXN1	C37	0.22u4/X5R5/6.3V/K	EXP A TXN1C
EXP A TXP2	C39	0.22u4/X5R5/6.3V/K	EXP A TXP2C
EXP A TXN2	C41	0.22u4/X5R5/6.3V/K	EXP A TXN2C
EXP A TXP3	C43	0.22u4/X5R5/6.3V/K	EXP A TXP3C
EXP A TXN3	C45	0.22u4/X5R5/6.3V/K	EXP A TXN3C
EXP A TXP4	C46	0.22u4/X5R5/6.3V/K	EXP A TXP4C
EXP A TXN4	C49	0.22u4/X5R5/6.3V/K	EXP A TXN4C
EXP A TXP5	C50	0.22u4/X5R5/6.3V/K	EXP A TXP5C
EXP A TXN5	C51	0.22u4/X5R5/6.3V/K	EXP A TXN5C
EXP A TXP6	C52	0.22u4/X5R5/6.3V/K	EXP A TXP6C
EXP A TXN6	C54	0.22u4/X5R5/6.3V/K	EXP A TXN6C
EXP A TXP7	C57	0.22u4/X5R5/6.3V/K	EXP A TXP7C
EXP A TXN7	C58	0.22u4/X5R5/6.3V/K	EXP A TXN7C
EXP A TXP8	C60	0.22u4/X5R5/6.3V/K	EXP A TXP8C
EXP A TXN8	C61	0.22u4/X5R5/6.3V/K	EXP A TXN8C
EXP A TXP9	C62	0.22u4/X5R5/6.3V/K	EXP A TXP9C
EXP A TXN9	C63	0.22u4/X5R5/6.3V/K	EXP A TXN9C
EXP A TXP10	C64	0.22u4/X5R5/6.3V/K	EXP A TXP10C
EXP A TXN10	C66	0.22u4/X5R5/6.3V/K	EXP A TXN10C
EXP A TXP11	C66	0.22u4/X5R5/6.3V/K	EXP A TXP11C
EXP A TXN11	C67	0.22u4/X5R5/6.3V/K	EXP A TXN11C
EXP A TXP12	C68	0.22u4/X5R5/6.3V/K	EXP A TXP12C
EXP A TXN12	C70	0.22u4/X5R5/6.3V/K	EXP A TXN12C
EXP A TXP13	C72	0.22u4/X5R5/6.3V/K	EXP A TXP13C
EXP A TXN13	C73	0.22u4/X5R5/6.3V/K	EXP A TXN13C
EXP A TXP14	C74	0.22u4/X5R5/6.3V/K	EXP A TXP14C
EXP A TXN14	C75	0.22u4/X5R5/6.3V/K	EXP A TXN14C
EXP A TXP15	C77	0.22u4/X5R5/6.3V/K	EXP A TXP15C
EXP A TXN15	C78	0.22u4/X5R5/6.3V/K	EXP A TXN15C



Title			
PCI EXPRESS * 16			
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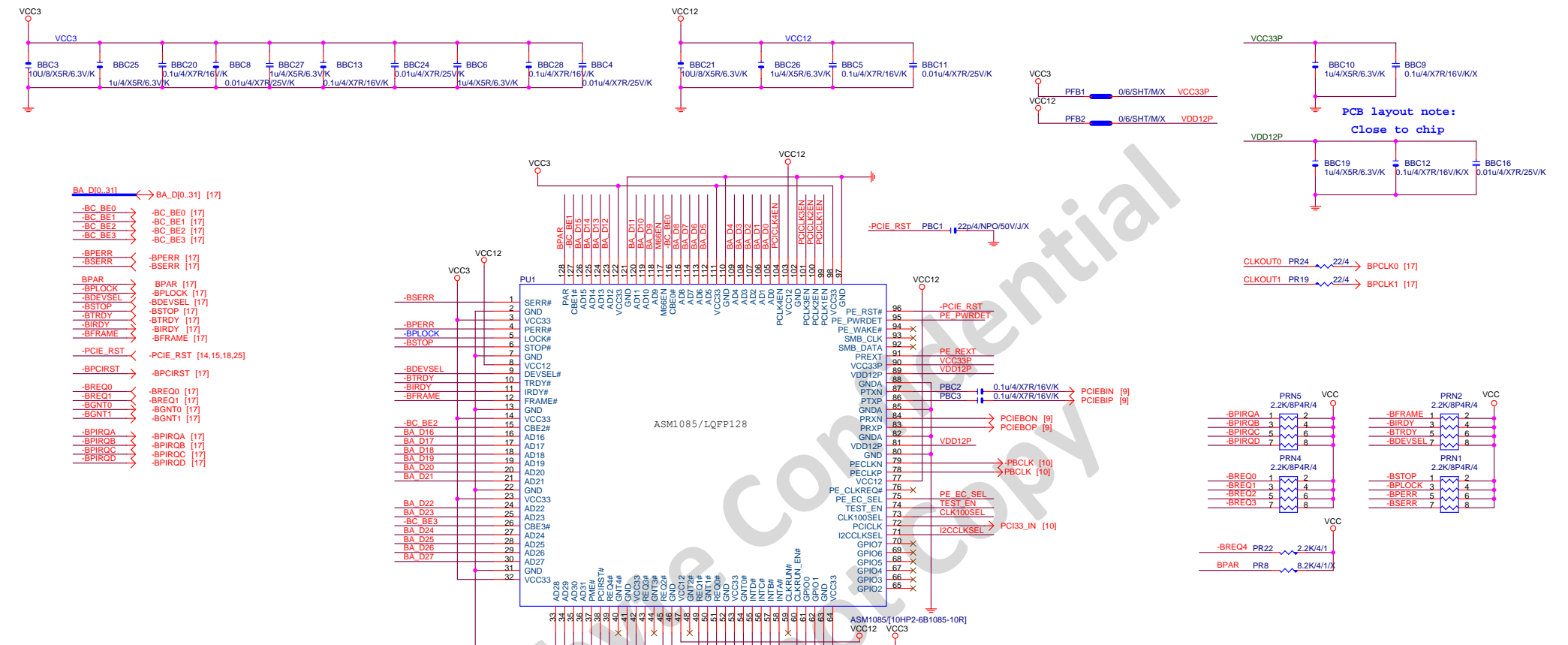
✕ B81 PRSNT2\*

PCI-E/16X-65P/BU/RIGHT PUSH

Gigabyte Technology			
Title			
PCI EXPRESS X 4 PORT			
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# PCIE TO PCI



## CLK100SEL Strapping Set

CLK100SEL	H	
PCie CLK	100M +/-N%	100ML +/-N%
PCICLK_IN	X	33M
PCICLK0	33M +/-N%	33M

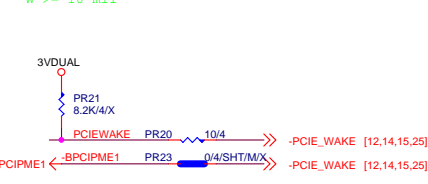
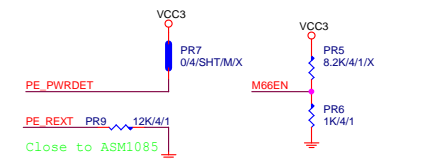
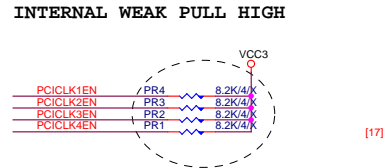
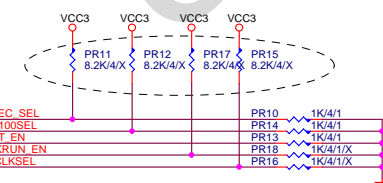
PE\_EC\_SEL-  
 "H" for Express Card mode  
 "L" for PCIe Riser Card mode

CLK100SEL-  
 "H" for PCLK input only  
 "L" for PCLK & PCICLK input

TEST\_EN-  
 "H" for Test Mode Enable  
 "L" for Test Mode Disable

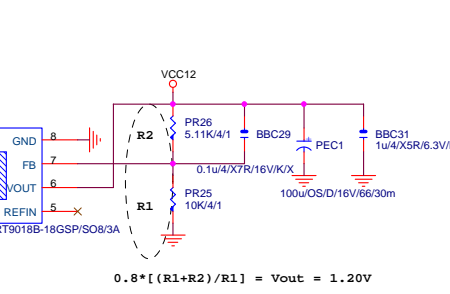
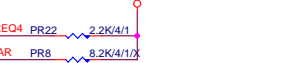
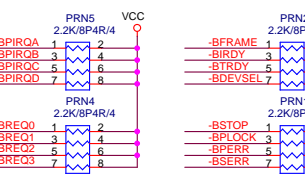
-CLKRUN\_EN-  
 "H" for CLKRUN Mode Disable  
 "L" for CLKRUN Mode Enable

I2CCLKSEL-  
 "H" is 135KHz I2CCLK  
 "L" is 67.5KHz I2CCLK



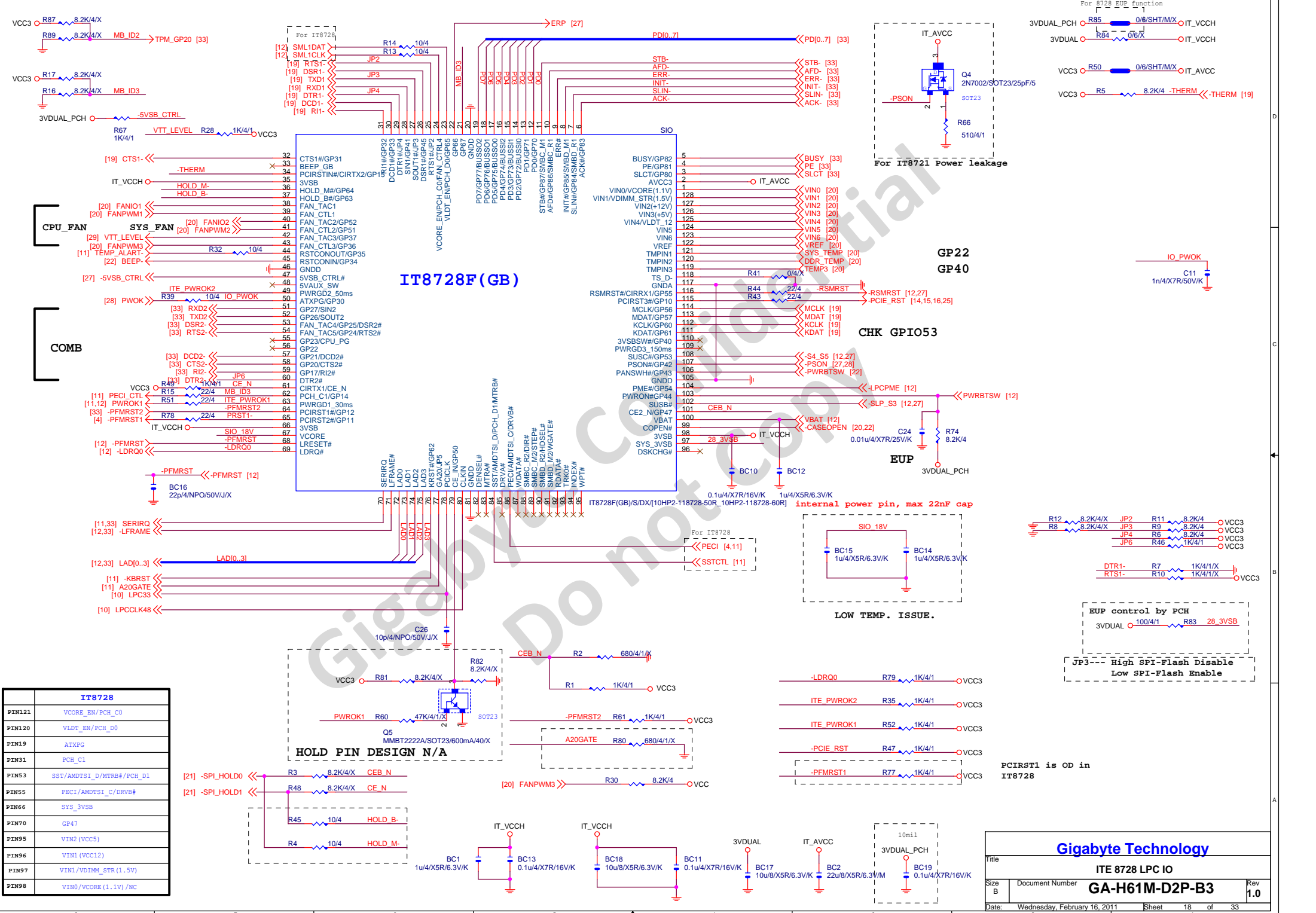
PCB layout note:  
 Close to chip

CLKOUT0 PR24 22/4 → BPCLK0 [17]  
 CLKOUT1 PR19 22/4 → BPCLK1 [17]

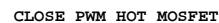
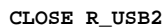
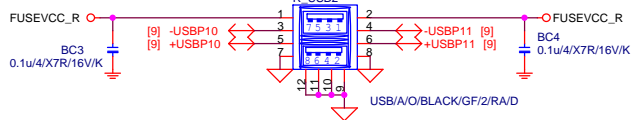
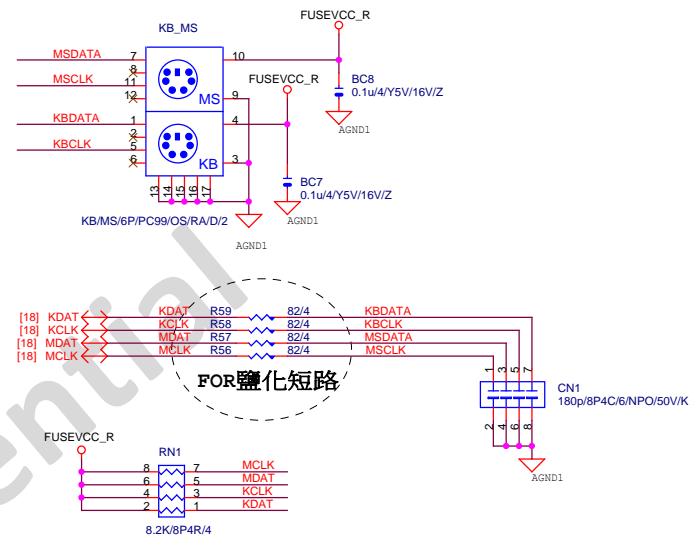
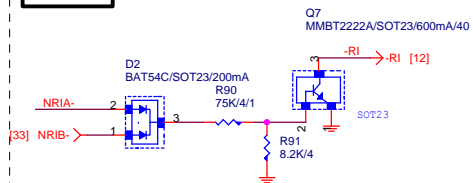
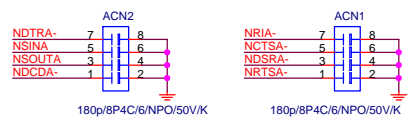


$$0.8 * [(R1+R2)/R1] = V_{out} = 1.20V$$

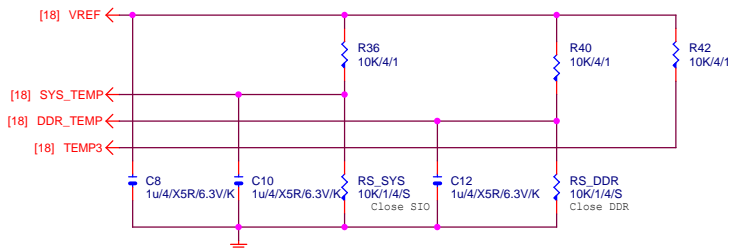




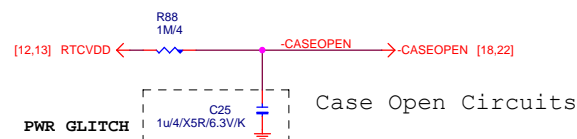
IT8728	
PIN121	VCORE_EN/PCH_C0
PIN120	VLDT_EN/PCH_D0
PIN19	ATXPG
PIN31	PCH_C1
PIN53	SST/AMDTSI_D/MTRB#/PCH_D1
PIN55	PEC1/AMDTSI_C/DRV#
PIN66	SYS_3VSB
PIN70	GP47
PIN95	VIN2 (VCC5)
PIN96	VIN1 (VCC12)
PIN97	VIN1/VDIMM_STR (1.5V)
PIN98	VIN0/VCORE (1.1V) /NC



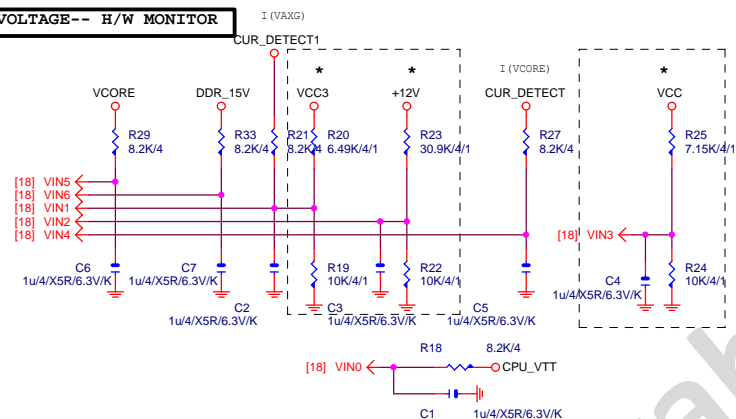
## TEMP H/W MONITOR



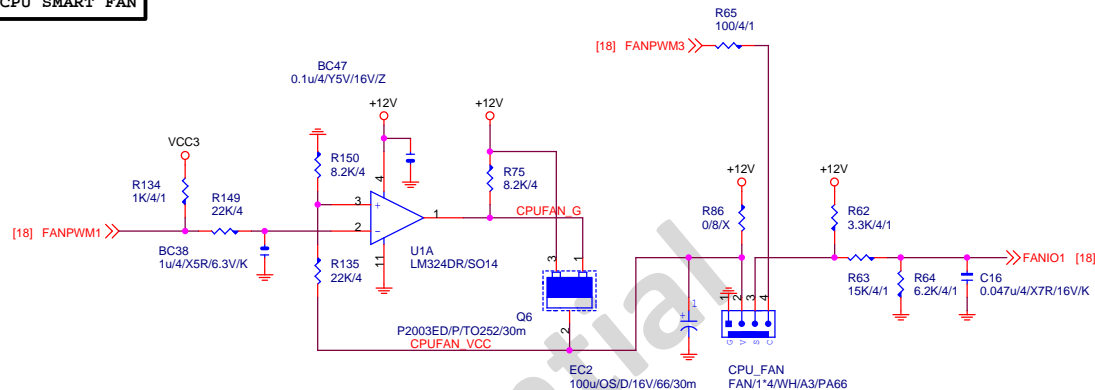
## CASE OPEN



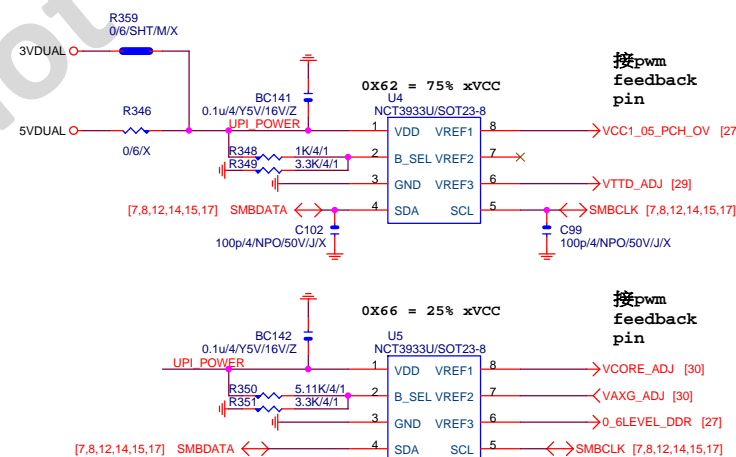
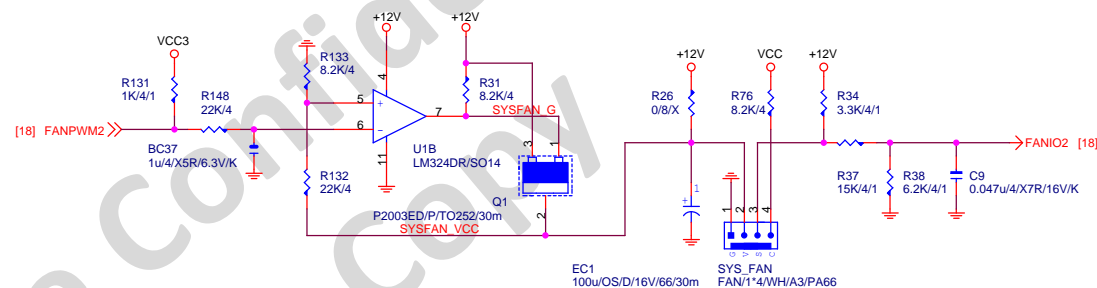
## VOLTAGE-- H/W MONITOR



## CPU SMART FAN



## SYS SMART FAN



Gigabyte Technology

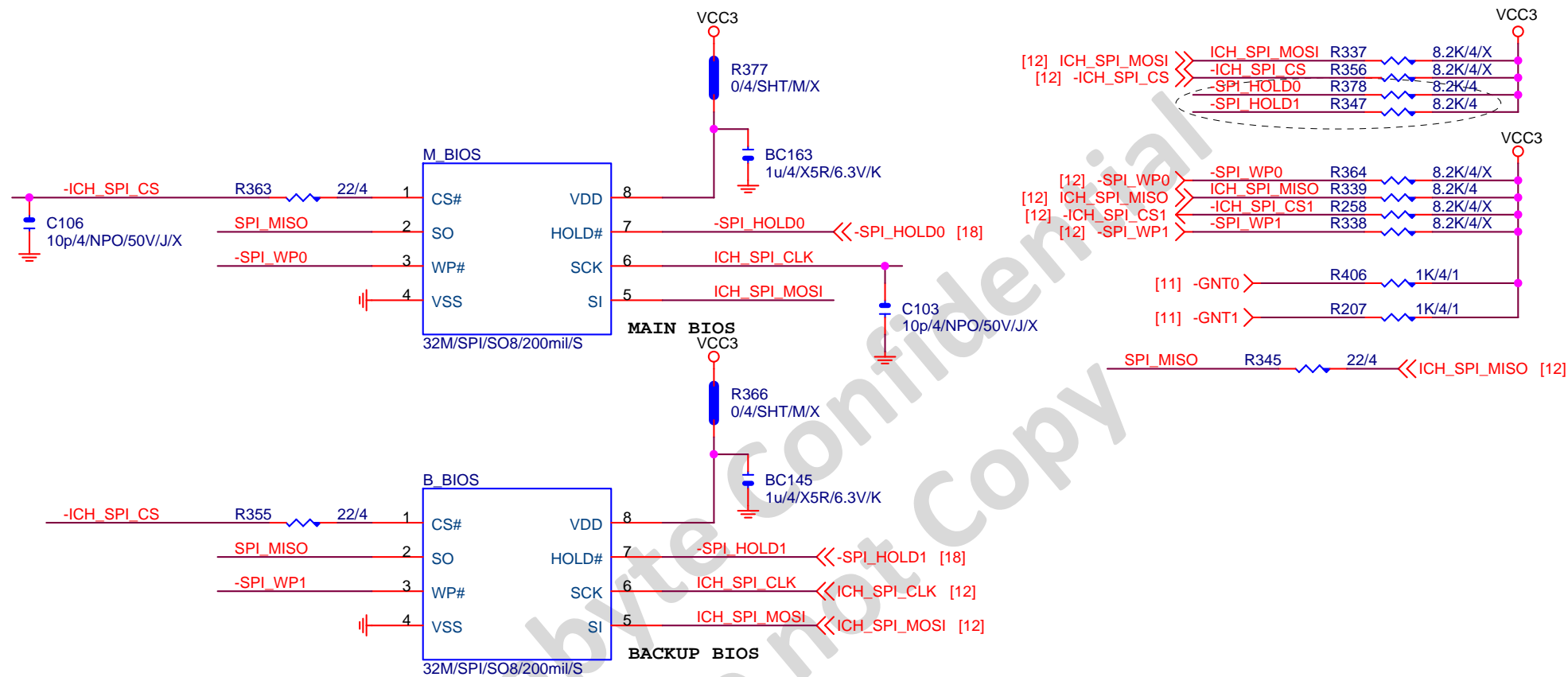
HWM,FAN CTRL,OV

GA-H61M-D2P-B3

Rev 1.0

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## DUAL BIOS



## B65使用64M BIOS

使用H67暫用32M

## H61使用32M BIOS

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

```

1 means floating
0 means PD 1K

```

## ***Gigabyte Technology***

Title
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## DUAL BIOS

Size  
A

Document Number
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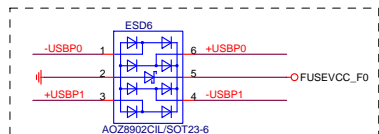
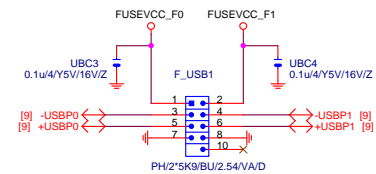
**GA-H61M-D2P-B3**

Rev	1.0
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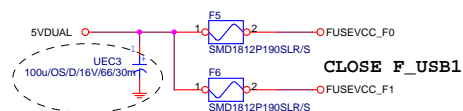
Date: Wednesday, February 16, 2011

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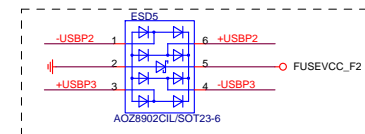
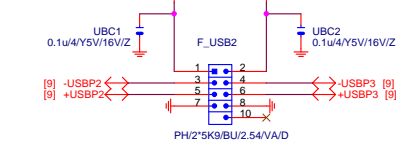
# FRONT USB1



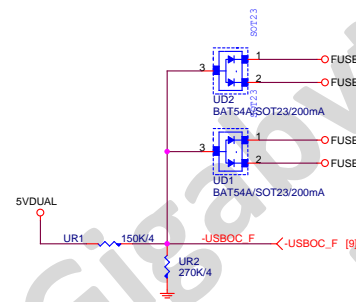
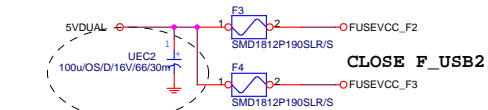
Close to connector



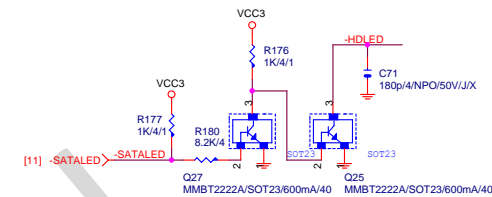
# FRONT USB2



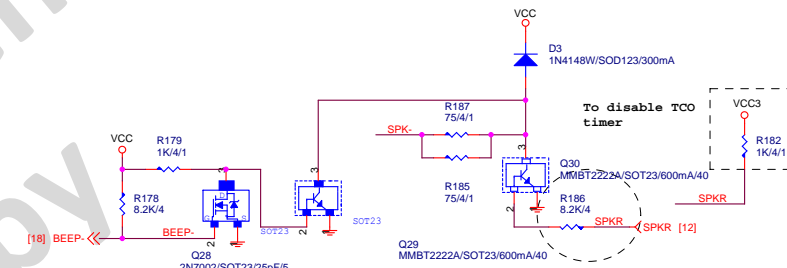
Close to connector



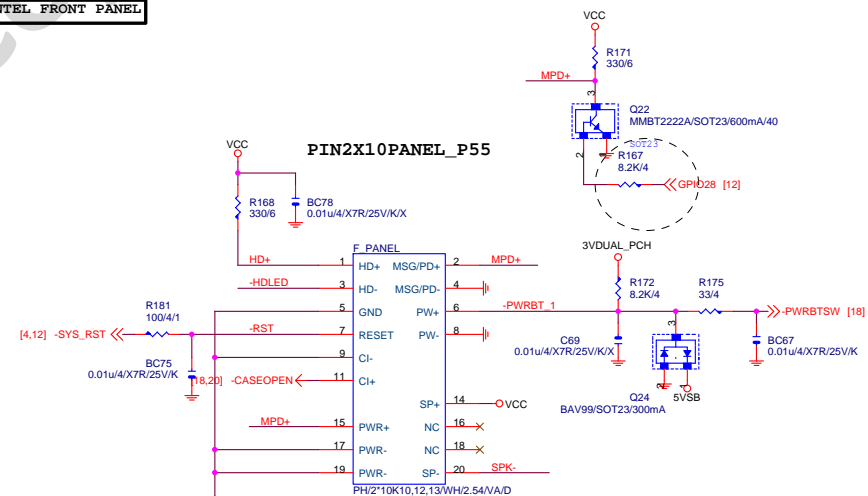
# SATA LED



# SPKR



# INTEL FRONT PANEL

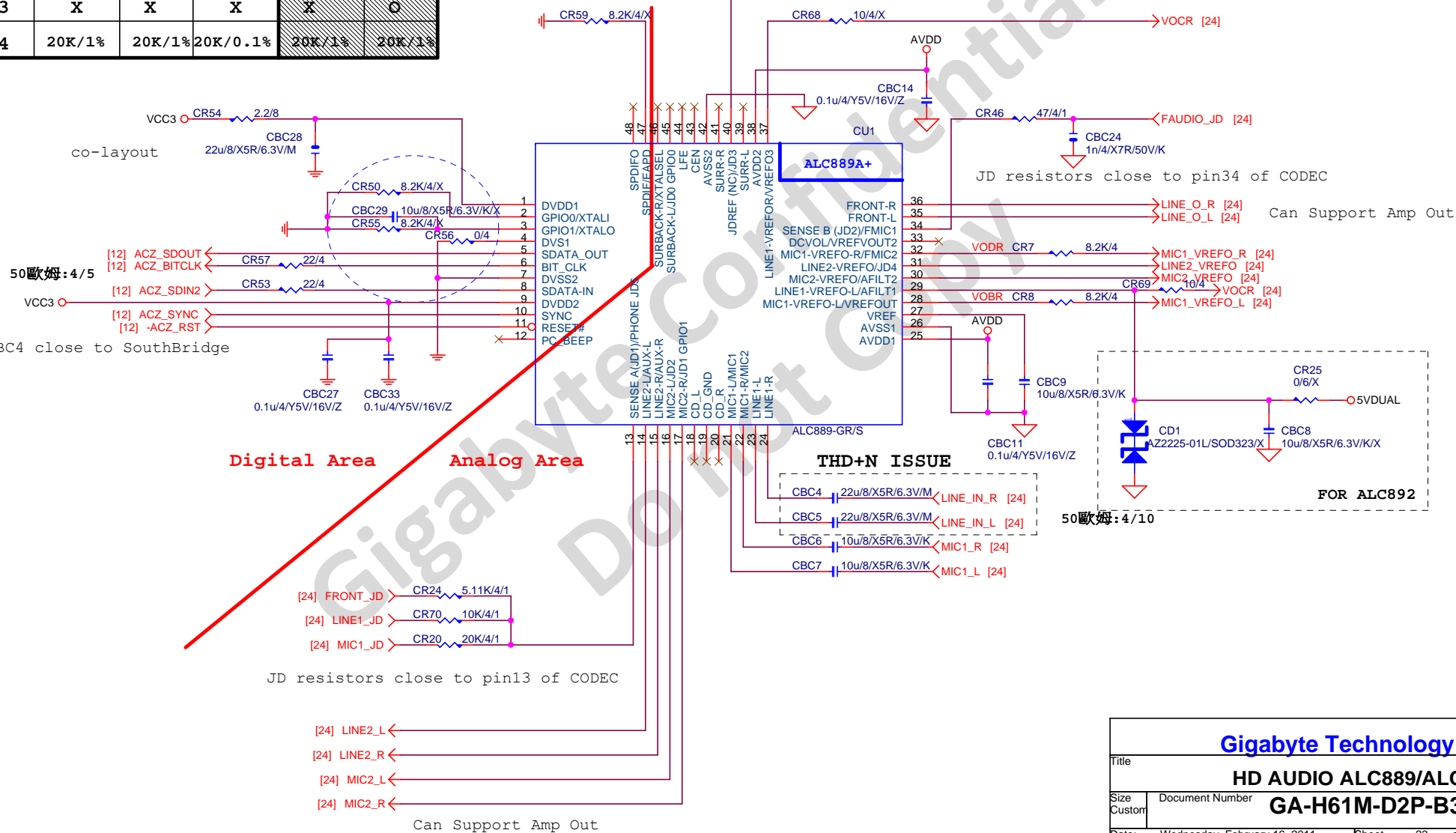


Gigabyte Technology

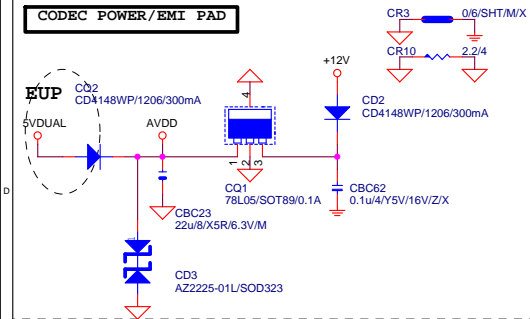
Title			
FP,F_USB,USB PWR,SPKR,SATA LED			
Size	Document Number	Rev	
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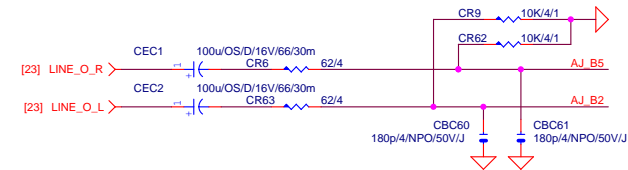
	ALC888B	ALC888-VA	ALC889A	ALC888-VD	ALC892
CR59	X	O	O	O	O
CR53,58	X	X	O	X	X
CR56	O	O	O	O	X
CR63	X	X	X	X	O
CR34	20K/1%	20K/1%	20K/0.1%	20K/1%	20K/1%



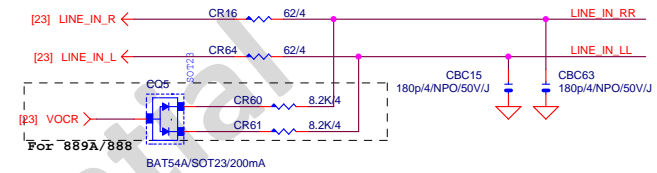
## CODEC POWER/EMI PAD



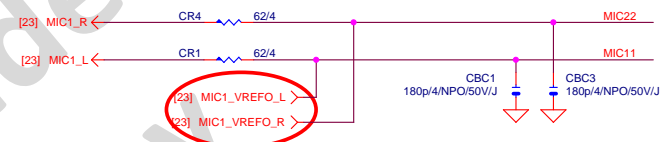
LINE-OUT



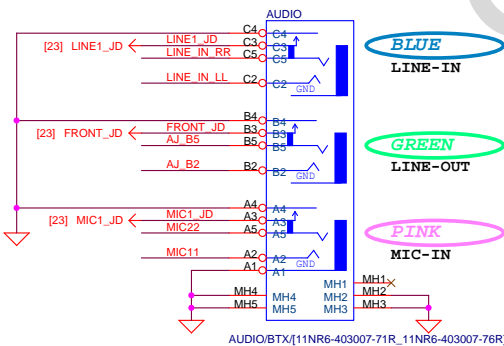
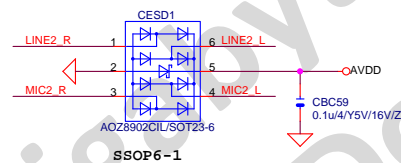
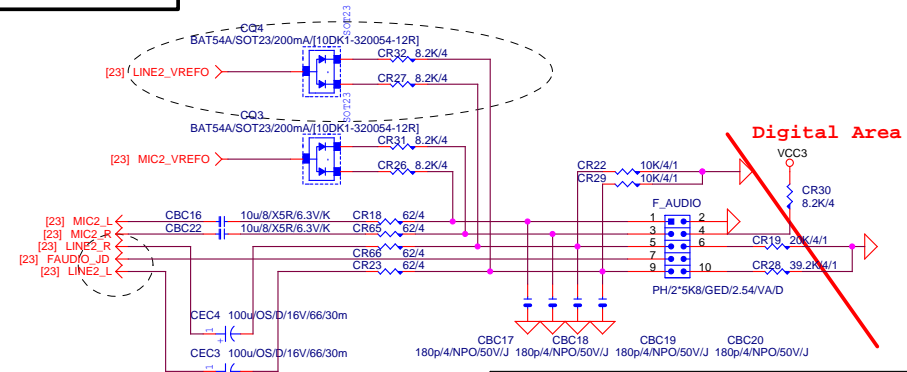
**LINE-IN**



## MIC-IN



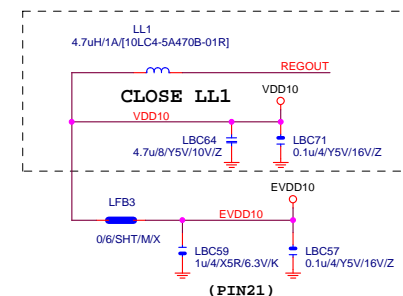
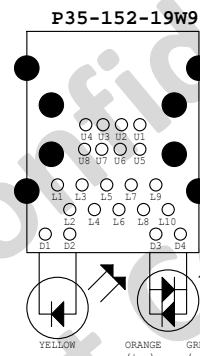
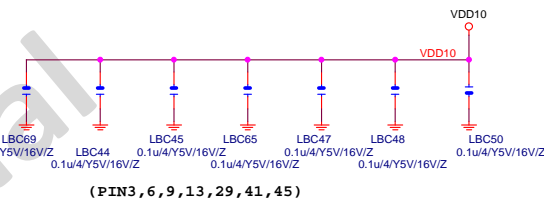
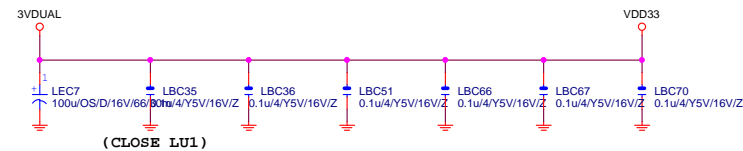
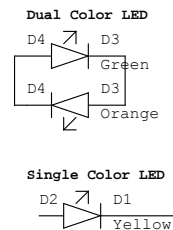
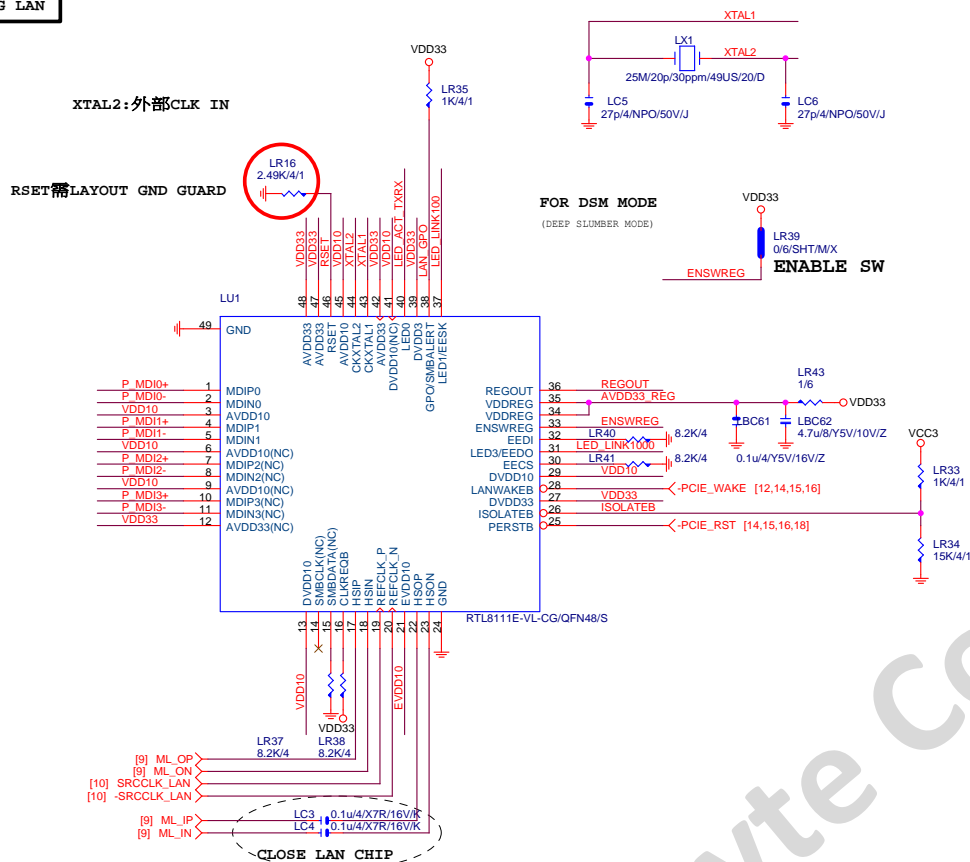
AZALIA JACK

**AZALIA FRONT PANE**

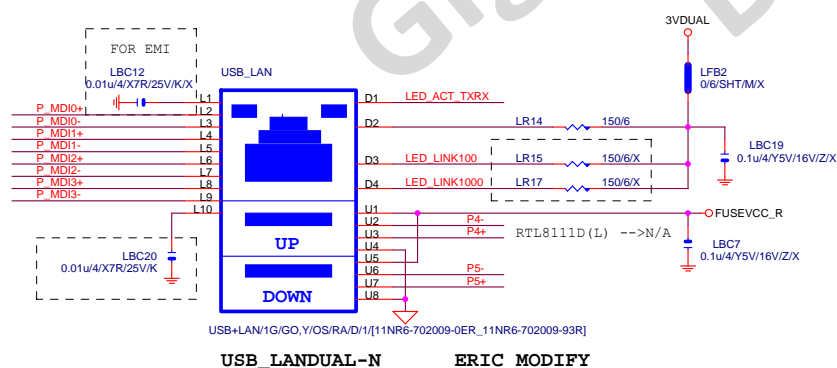
## Gigabyte Technology

Title			
AUDIO JACK			
Size Custom	Document Number	GA-H61M-D2P-B3	Rev 1.0
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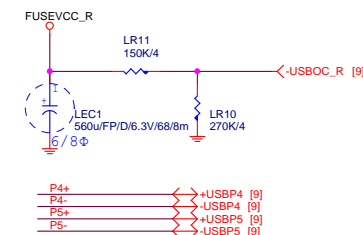
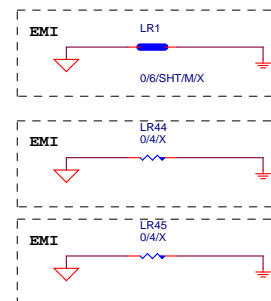
## PCIE-1G LAN

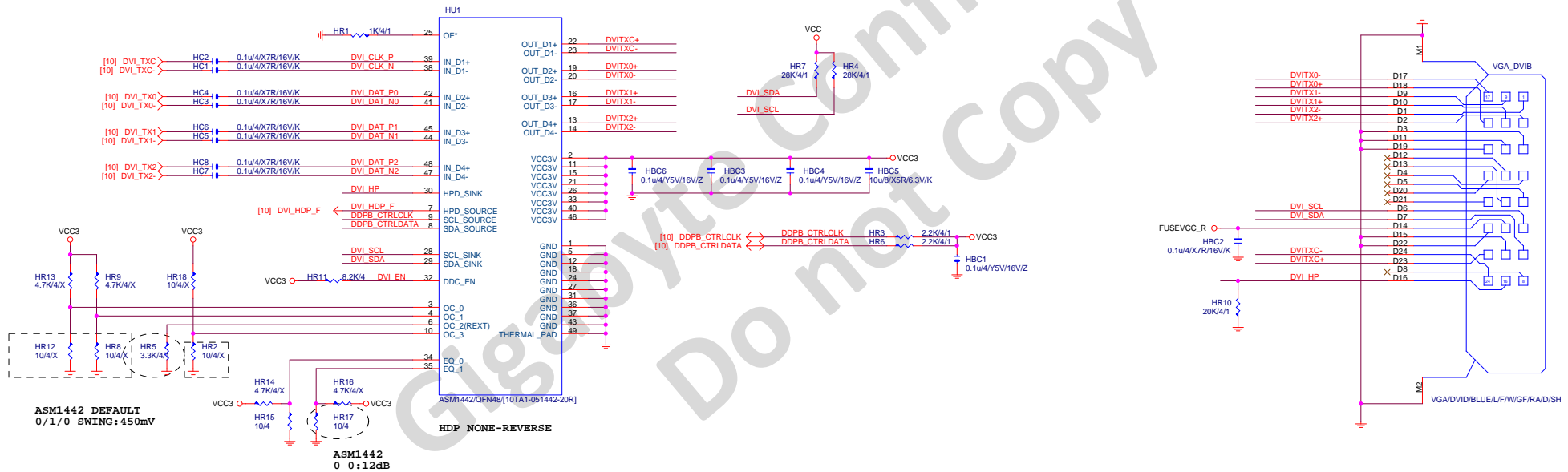


## USB\_LAN\_CONNECTOR

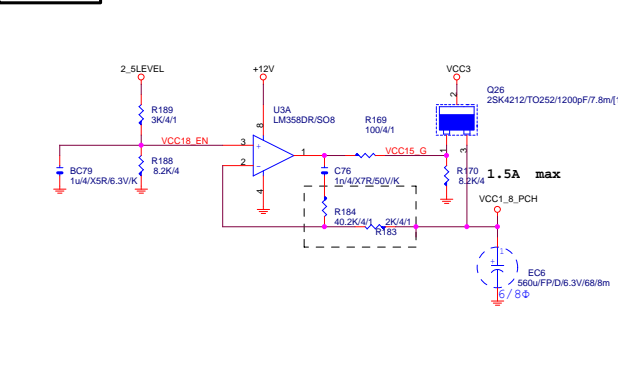


USB\_LAN

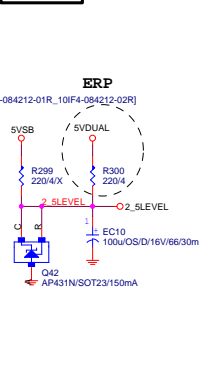




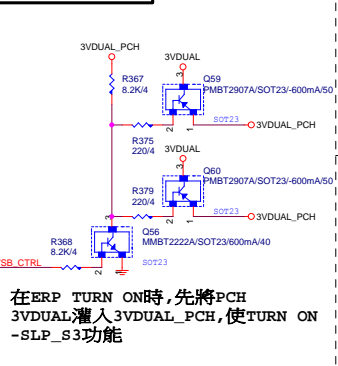
VCC1\_8\_PCH



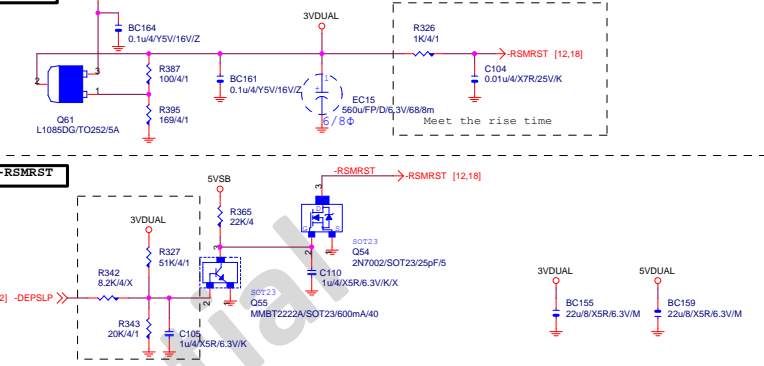
2\_5LEVEL



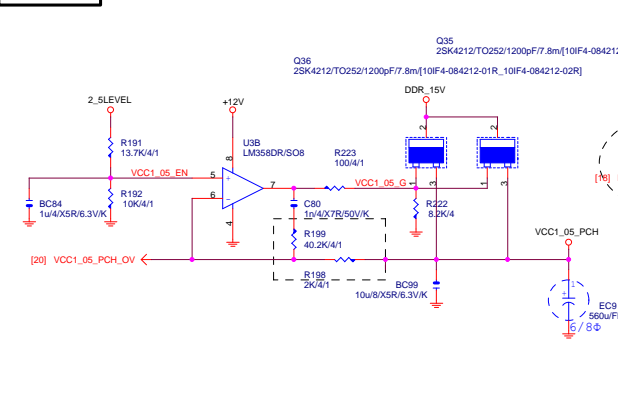
FIX ERP 5VSB DROP



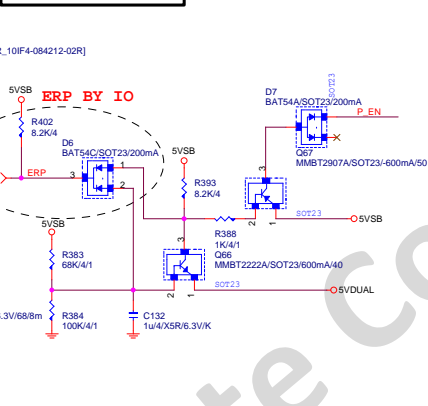
3VDUAL



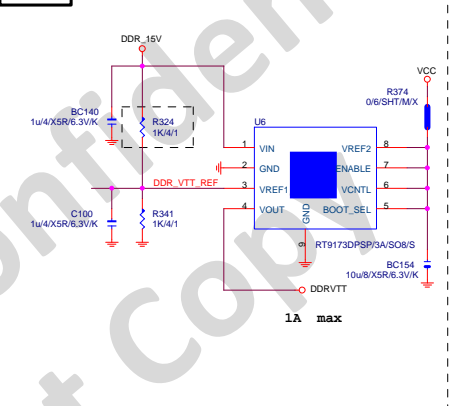
VCC1\_05\_PCH



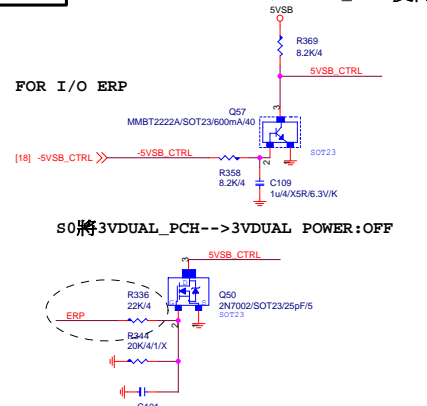
5VDUAL SHORT PROTECT



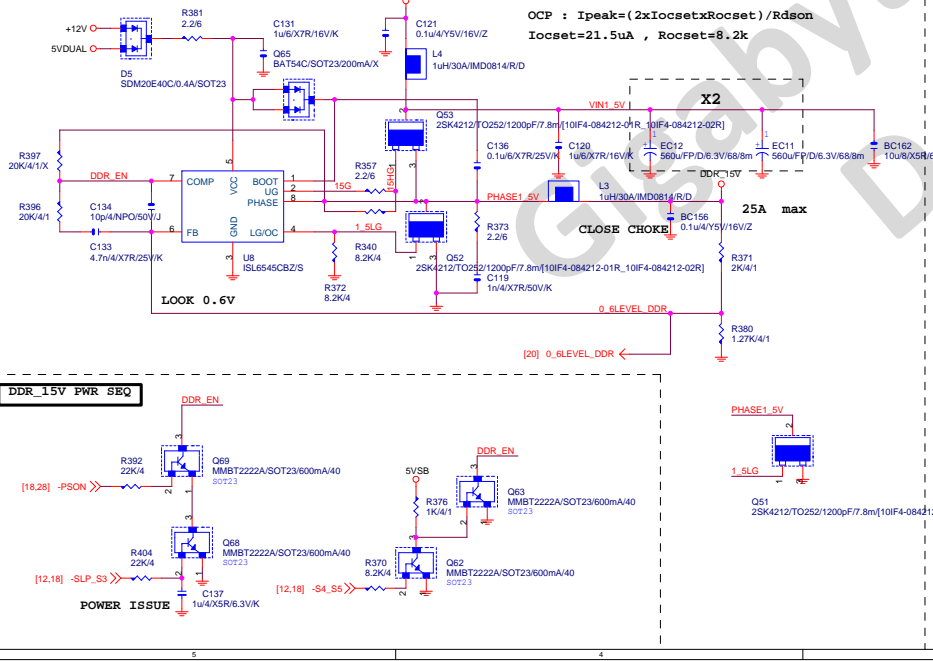
DDRVTT



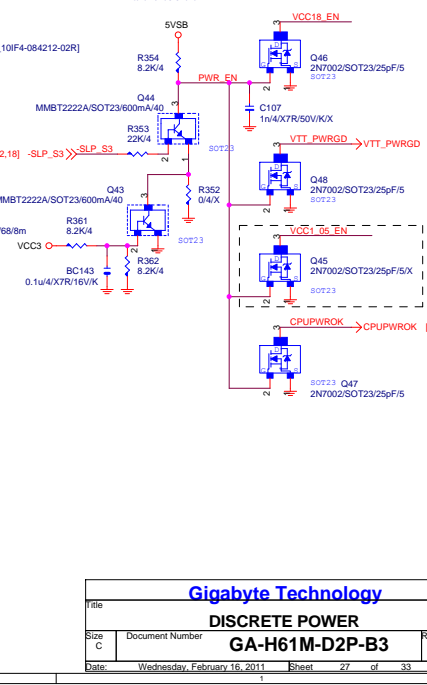
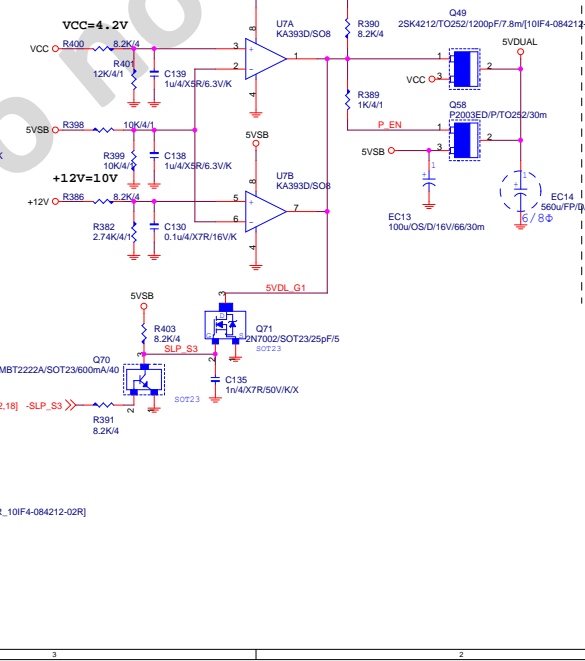
PWR SEQ



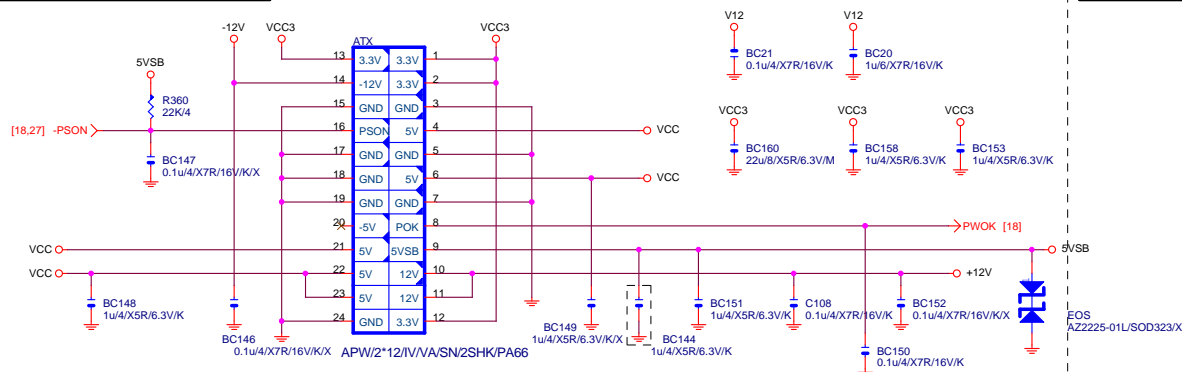
DDR\_15V



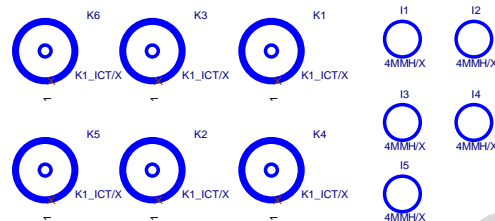
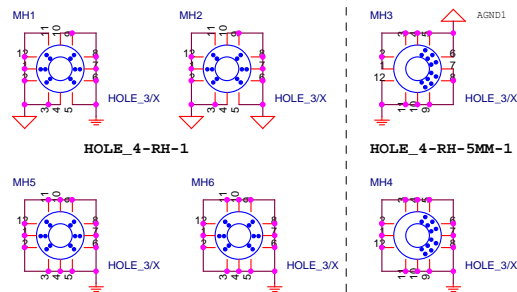
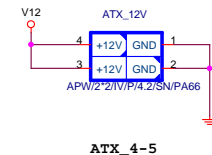
5VDUAL



ATXX24 POWER CONNECTOR

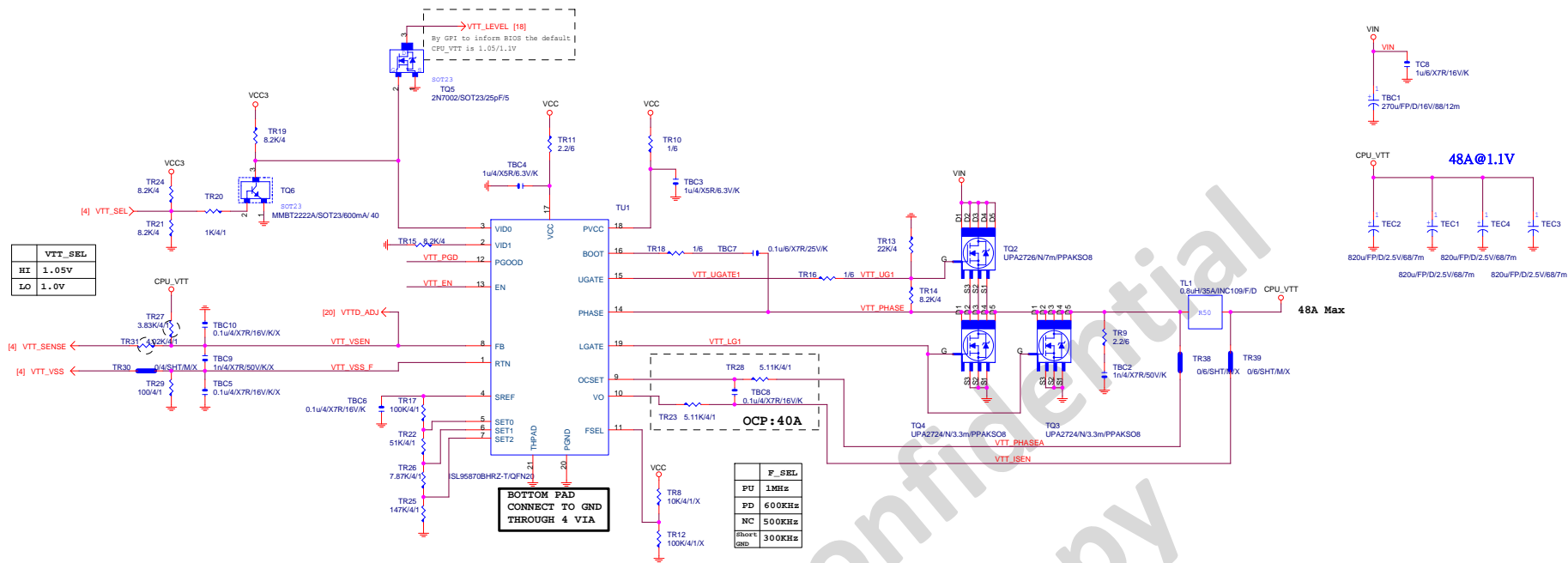


**ATXX4 POWER CONNECTOR**

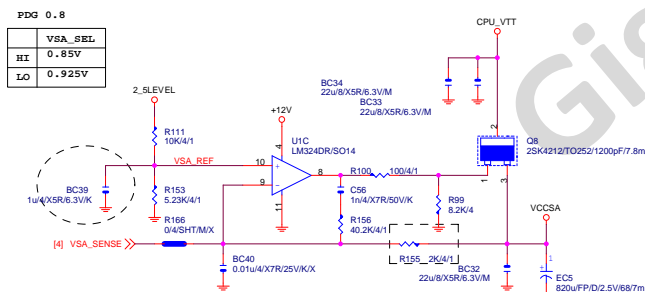


```
| To prevent the 5VSB  
| under loading when  
| boot
```

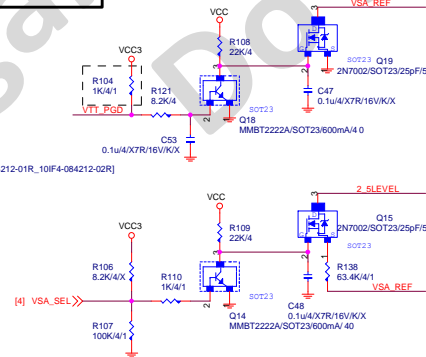
## CPU\_VTT



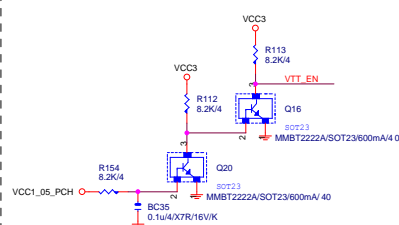
## VCCSA



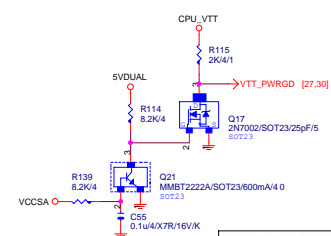
## VCCSA PWR SEQ



## CPU\_VTT PWR SEQ



## VTT\_PWRGD



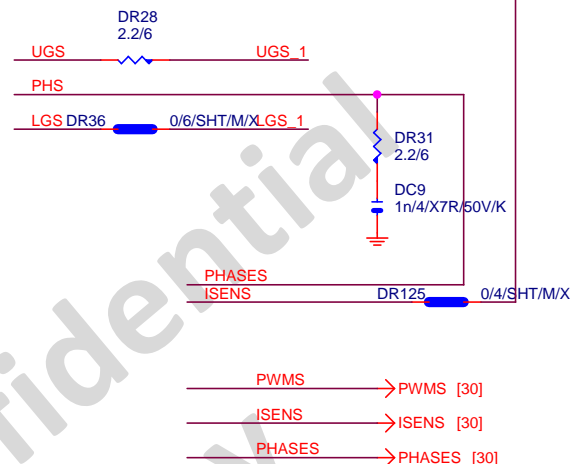
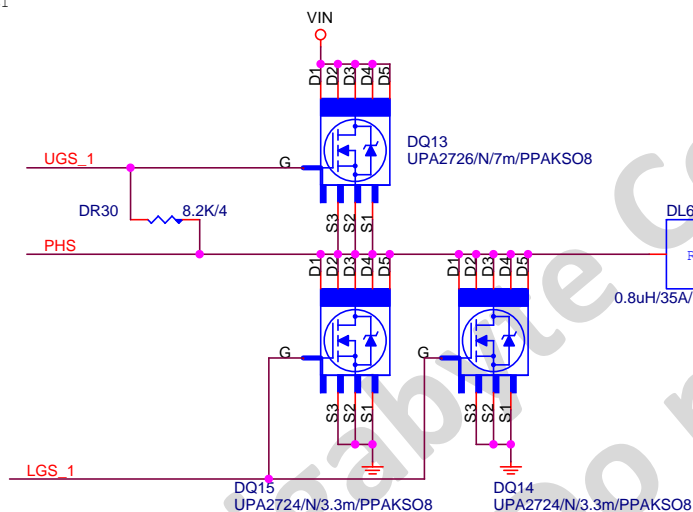
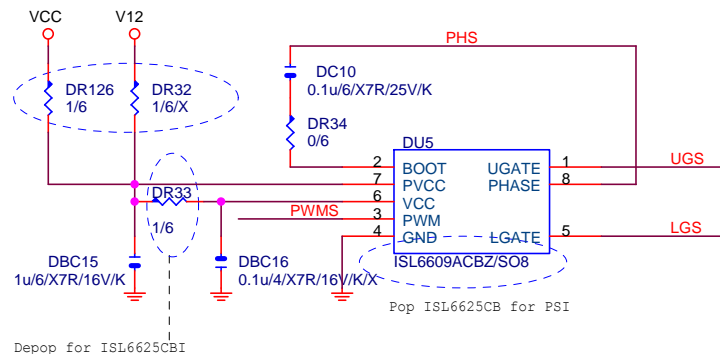




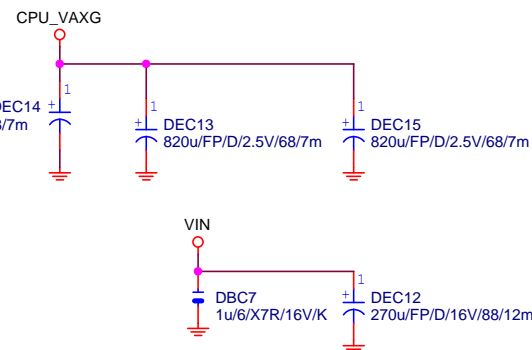
# VAXG

ISL6612 use +12V  
ISL6609 use VCC

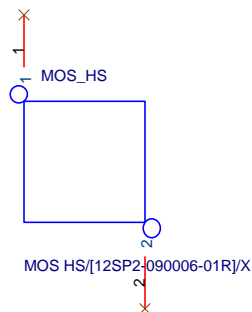
ISL6612 use 1 ohm  
ISL6609 use 0 ohm



PWMS → PWMS [30]  
ISENS → ISENS [30]  
PHASES → PHASES [30]



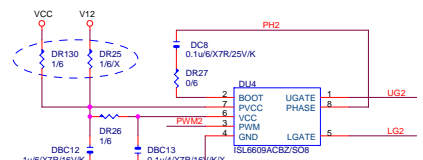
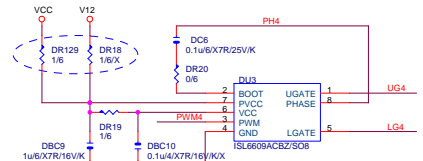
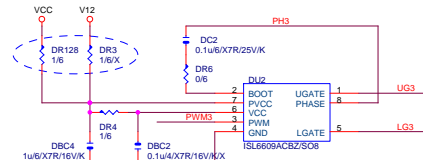
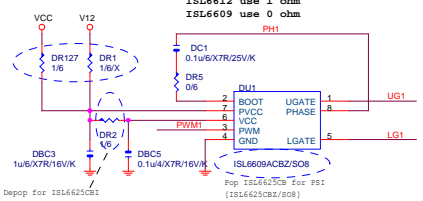
# MOS HEATSINK



**Gigabyte Technology**

Title		
CPU CORE VR-2		
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ISL6612 use +12V  
ISL6609 use VCC

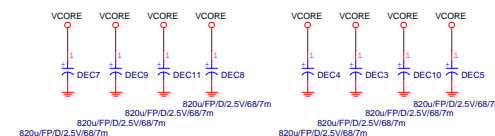
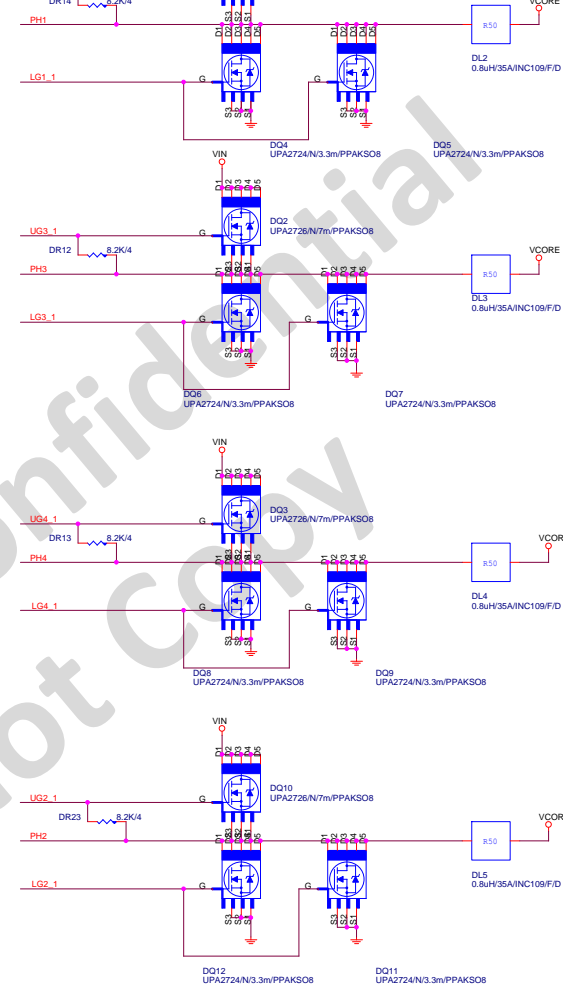
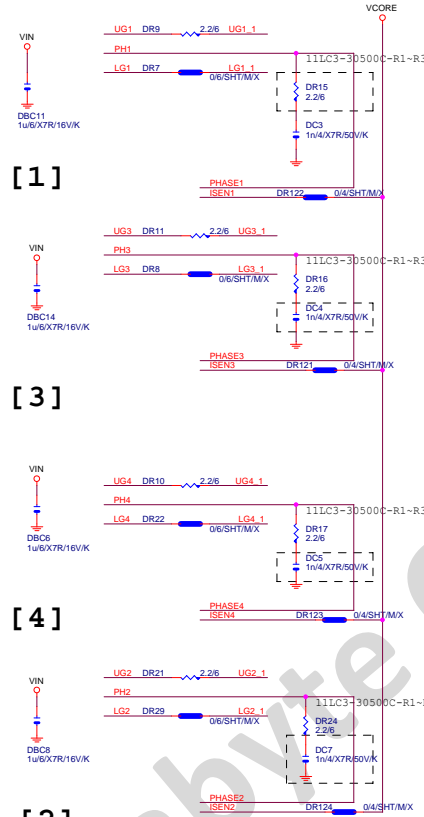


[1]

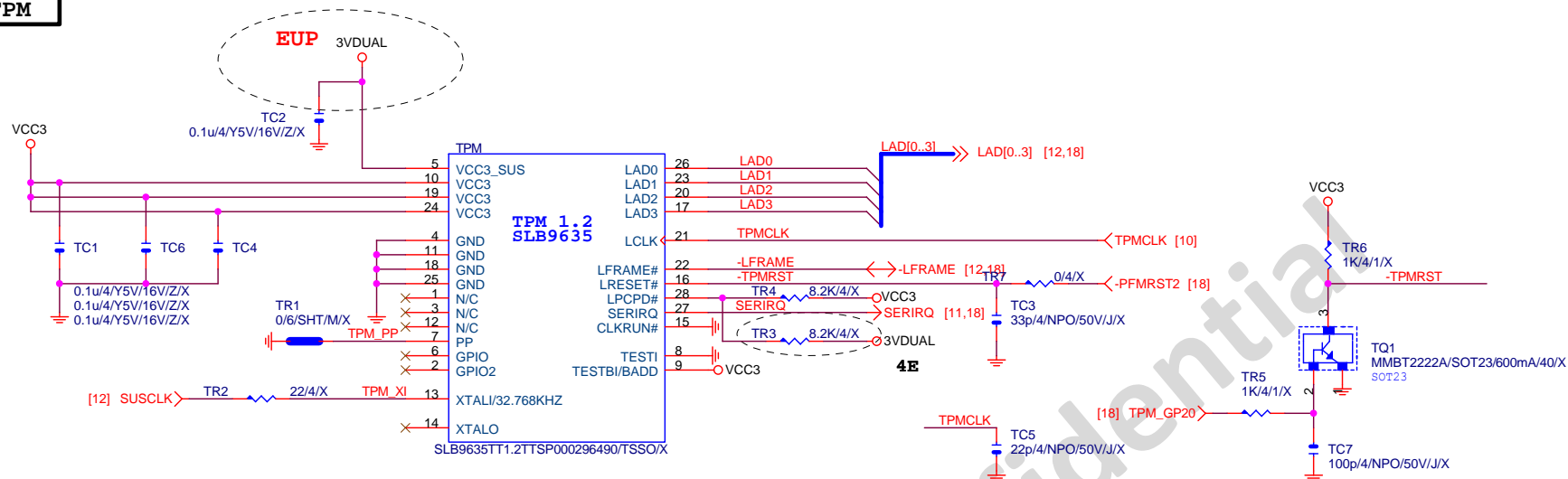
[3]

[4]

[2]

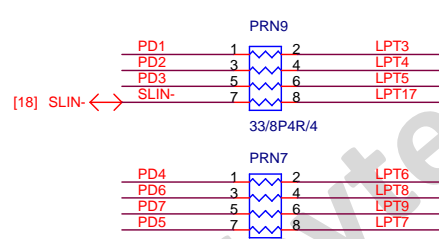
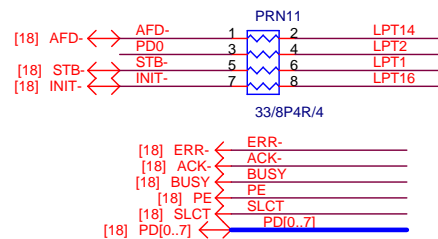


## TPM



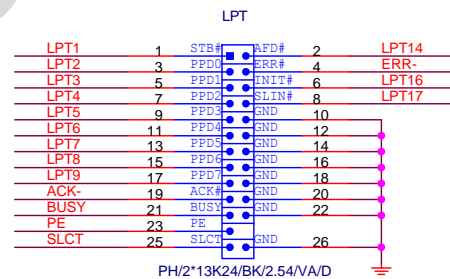
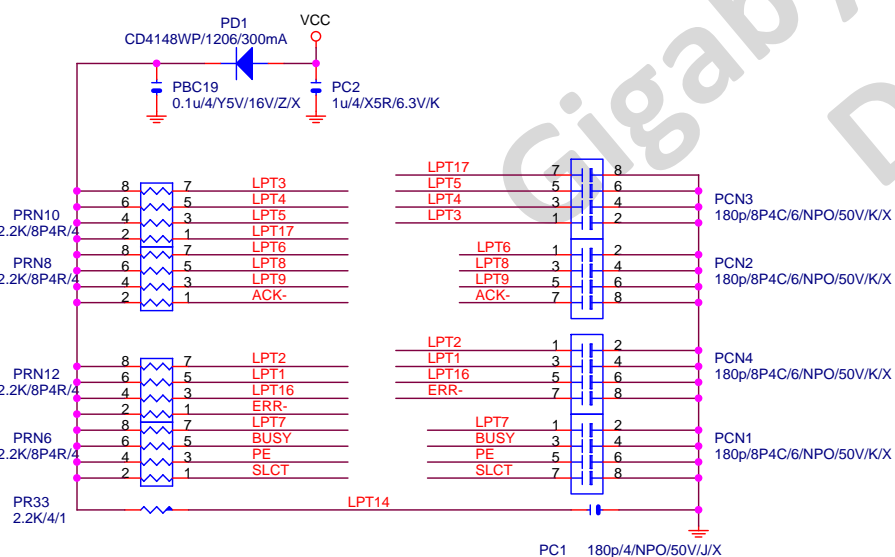
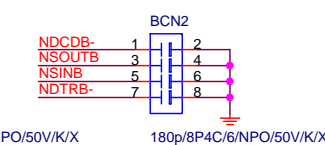
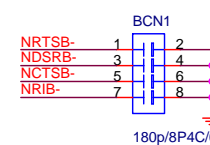
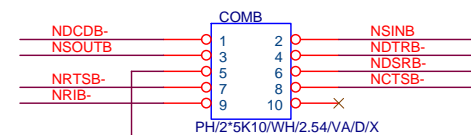
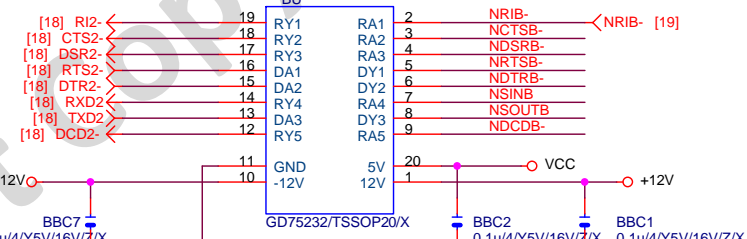
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LPT PORT



COMB

N/A



PIN2X13\_LPT-CUT24

## Gigabyte Technology

TPM,COMB,LPT

**GA-H61M-D2P-B3**

Rev	
1.0	